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(54) Data processing circuit, microcomputer, and electronic equipment

Datenverarbeitungsschaltung, Mikrocomputer und elektronische Einrichtung

Circuit de traitement de données, micro-ordinateur et dispositif électronique

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Description

Background of the Invention

Field of the Invention

[0001] This invention relates to a data processing circuit, a microcomputer incorporating this data processing circuit, and electronic equipment that is constructed by using this microcomputer.

Description of Related Art

[0002] In the prior art a RISC microcomputer that is capable of manipulating 32-bit data uses fixed-length instructions that are 32 bits wide. This is because the use of fixed-length instructions enables a reduction in the time required for decoding the instructions in comparison with the use of variable-length instructions, and it also makes it possible to reduce the size of the circuitry of tne microcomputer.

[0003] However, even with a 32-bit microcomputer, it isn't always necessary to use the full 32 bits. Thus, if all of the instructions are written as 32-bit instructions, many of them will contain unused portions so that memory will be used inefficiently.

[0004] The present inventors have investigated the idea of a microcomputer that handles fixed-length instructions of a bit width that is narrower than that of the executable data, to improve the usage efficiency without making the control circuitry more complicated.

[0005] However, simply cutting 32-bit fixed-length instructions to fit into a fixed 16-bit length, for example, causes problems as described below.

[0006] An important feature of a RISC microcomputer is the use of general-purpose registers, whose contents have no preassigned meaning. For that reason, when a stack pointer is used, one of the general-purpose register is used as the stack pointer and an instruction that acts upon a general-purpose register is used to implement stack operation.

[0007] When coding a process that takes data specified by a memory address obtained by adding a predetermined offset to the stack pointer and transfers it to a predetermined register, using an instruction that acts upon a general-purpose register, for example, it is necessary to include within the object code of that instruction the offset, data specifying the predetermined register, and data specifying the register to be used as the stack pointer.

[0008] Thus, if an instruction that acts upon a general-purpose register is used when coding a process that acts upon the stack pointer, a large amount of data has to be specified in the object code, making it difficult to code the details of the instruction within a 16-bit fixed-length. Increasing the instruction length to 32 bits, for example, would result in a large number of instructions that do not particularly need the entire 32 bits, so that many instructions will contain unused portions, leading to a decrease in the efficiency with which memory is used.

[0009] In addition, increasing the instruction length will also increase the amount of memory required for storing such instructions, so it is preferable from the point of view of efficient use of memory to not only use fixed-length instructions, but also make the instructions as short as possible.

[0010] When a program is executed that was written in a language that secures a storage region for auto-variables linked to the stack pointer, such as programming language C, there are many instructions that act upon the stack pointer, so it is preferable to have efficient coding and execution of instructions that act upon the stack pointer.

[0011] In that case, it is therefore preferable to have an architecture that enables the coding and execution of instructions that are as short as possible, when executing a process that acts upon the stack pointer.

[0012] It has become common recently to incorporate general-purpose registers internally, particularly with a RISC CPU, to increase capabilities. Providing a large number of registers internally makes it possible for many processes to be executed rapidly within the CPU itself, without having to access memory. If such a large number of internal registers is provided, a large number of registers have to be saved during the process of register save and restoration when an interrupt is processed or a subroutine is called.

[0013] The description now turns to a prior-art example of instructions that save and restore the contents of registers, frequently used when entering and leaving a subroutine, even within stack-related instructions.

[0014] The instruction set of a microcomputer usually has instructions for saving and restoring the contents of registers in the CPU to and from a stack provided in memory. These are either dedicated instructions or instructions that address registers indirectly.

[0015] In the Intel 80386 chip, push, pusha, and pushad instructions are available for writing the contents of registers to the stack, and pop, popa, and popad instructions are available for returning data from the stack to registers.

[0016] When the contents of a register are written to the stack by the push instruction, the register has to be specified as an operand, such as 'push EAX.' This example concerns a 32-bit register EAX. If the contents of registers EAX, ECX, EDX, and EBX are all to be written to the stack, this push instruction must be repeated, as follows:

```
push EAX
push ECX
push EDX
push EBX
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[0017] If such push and pop instructions are used for each of the registers, the size of the object code increases and a large number of program execution steps is required, leading to delays in the execution time or processing of the program.

[0018] That is why the pusha or pushad instruction is used to write the contents of all eight of the general-purpose registers of the 80386 to the stack. pusha operates on the lower 16 bits of each of the eight registers, and pushad operates on the entire 32 bits. The use of pusha and pushad can remove the need to repeat the push instruction eight times.

[0019] The pop, popa, and popad instructions act in a similar manner.

[0020] Disadvantages of repeating the push instruction include the increased length of program code and the delays in execution caused by executing a fetch for each instruction. From this point of view, the pusha and pushad instructions provide a large improvement when writing the contents of all eight registers to the stack. However, this is not an advantage when writing fewer than the eight registers, such as four or six registers.

[0021] In other words, if the pusha, pushad, popa, and popad instructions of the 80386 operate upon all of the registers, instructions with delayed cycle lengths must be used when there is no need to save and restore the contents of all of the registers. In such a case, one instruction will suffice, but this gives rise to a problem in that the execution cycle of that instruction takes too long.

[0022] Similar saving and restoration of the program counter is necessary when program flow branches to a subroutine and returns from the called routine, using instructions such as the call instruction and ret instruction. With a RISC CPU of the prior art, these processes are implemented by software. In other words, the program counter is saved and restored by executing assembler instructions (object code) that declare these processes. This leads to an increase in object code of the call and ret instructions, and the execution of a fetch for each instruction makes the execution speed sluggish.

[0023] The document J.F. WAKERLY: "Micro-computer Architecture and Programming", 1981, JOHN WILEY & SONS, INC. NEW YORK, US XP-002084219 describes the MOTOROLA 68000 microprocessor architecture that includes features corresponding to those in the pre-characterizing portion of claims 1 and 2. WO 9608767 A discloses a microcontroller system capable of transferring data between a memory stack and a plurality of general-purpose registers listed in an instruction in a single instruction cycle. A single instructions causing data for a plurality of registers to be pushed or poped to or from the stack include, inter alia, a binary list of the registers involved.

Summary of the Invention

[0024] An objective of this invention is to provide a data processing circuit, microcomputer, and electronic equipment having an architecture that enables efficient coding of processes that act upon the stack pointer within a short instruction length, for execution.

[0025] Another objective of this invention is to provide a data processing circuit, microcomputer, and electronic equipment that enables efficient coding of processes that save and restore the contents of registers, with fast processing of interrupts and subroutine calls and returns.

[0026] These objects are achieved by a data processing circuit as daimed in claims 1 and 2 and the preferred embodiments defined in the dependent claims.

[0027] In accordance with the invention it is made possible to implement the saving to the stack of the contents of a plurality of registers specified by linked sequential values and the restoration of data to a plurality of registers specified by linked sequential values, using only a count means and a simple sequence controller. Since this makes it possible to provide a data processing circuit with a small number of gates, this invention can be applied to one-chip microcomputers or the like.

[0028] When there are plural general-purpose registers, there are usually addresses for specifying these registers. A preferred embodiment of the invention specifies these registers by register number, in continuous sequence from 0 to n-1.

[0029] This aspect of the invention makes it possible to execute at least one of a push or pop of data between memory and a plurality of continuous registers from register 0 to the register with a final register number, by specifying any register number as the final register number. Therefore, the contents of registers can be saved and restored efficiency during the execution of a program having a structure that uses registers in sequence from register number 0.

[0030] According one embodiment, a subroutine could be such as an interrupt processing, exception processing, or debugging processing routine. Therefore, an instruction for branching to a subroutine could be such as an instruction

that calls a subroutine or the like, or a software interrupt instruction or software debugging interrupt instruction for branching to an interrupt processing, exception processing, or debugging processing routine. Similarly, a return instruction from the subroutine could be a return instruction such as from an interrupt processing, exception processing, and debugging processing routine.

[0031] It is usually necessary to save and restore the program counter when branching to a subroutine or returning from a subroutine.

[0032] This embodiment makes it possible to save and restore the program counter simultaneously with the execution of the instruction for branching to the subroutine and the instruction for returning from the subroutine. In other words, the data processing circuit of this aspect of the invention has a circuit structure that enables the saving and restoration of the program counter by either one of instruction, within an instruction for branching to a subroutine and a return instruction from the subroutine. There is therefore no need for instructions for the saving and restoration of the program counter, which is necessary when branching to a subroutine and returning therefrom, enabling a reduction in the number of instructions. This makes it possible to increase the speed of processing during a branch to another routine, such as subroutine call and return, without wasting cycles.

[0033] When a software interrupt instruction is generated, for example, it is necessary to save and restore the processor status register that holds the current state of the CPU or other data processing circuit. It is therefore preferable to perform this saving and restoration of the processor status register simultaneously with the execution of an instruction such as a software interrupt instruction. According to another embodiment, the data processing circuit uses instructions of a RISC.

[0034] A RISC data processing circuit is designed with the objectives of reducing the dimensions of the hardware and increasing the speed thereof. Thus, a RISC data circuit has many general-purpose registers. Reduction of the number of instructions is achieved by using only an instruction set which has universality.

[0035] Therefore, with a RISC data processing circuit, the stack pointer is allocated to a general-purpose register, and the processing uses an instruction set that acts upon this general-purpose register when manipulating the stack pointer. However, this method leads to an increased instruction length, so that memory is used inefficiently.

[0036] This aspect of the invention makes it possible to increase the efficiency with which memory is used by a RISC data processing circuit, by reducing the instruction length.

[0037] When the use of fixed-length instructions is compared with the use of variable-length instructions, it is possible to shorten time required for decoding the instructions and reduce the dimensions of the data processing circuit itself. To ensure that memory is used efficiently when fixed-length instructions are employed, by avoiding the creation of unused portions within instruction, it is preferable to have little variation in the number of bits necessary for each instruction, so that they are as short as possible.

[0038] Another embodiment of the invention makes it possible to reduce the length of instructions that act upon the stack pointer and thus tend to become too long. It is therefore possible to avoid the creation of unused portions within instructions, even when fixed-length instructions are employed, so that memory can be used more efficiently.

Brief Description of the Drawings

[0039]

Fig. 1	is a schematic view of the circuit structure of a CPU in accordance with a first embodiment of this invention;
Fig. 2	shows a register set of the CPU of this embodiment;
Fig. 3	is a view illustrative of the basic operation of the stack pointer;
Fig. 4	shows an example of the usage of a dedicated stack pointer instruction, as well as the usage state of the stack provided in memory and the state of the stack pointer;
Fig. 5	is a view illustrative of the process of transferring auto-variables in memory to registers;
Figs. 6A and 6B	show the bit fields of an SP-relative load instruction and a general-purpose load instruction;
Fig. 7	is a flowchart illustrative of the operation during the SP-relative load instruction for reading word data;
Fig. 8	is a flowchart illustrative of the operation during the SP-relative load instruction for writing word data;
Figs. 9A to 9F	show views illustrative of the usage state of the stack in memory and the state of the stack pointer during each routine of an executing program that extends over a plurality of routines;
Figs. 10A and 10B	show the bit fields of a stack pointer move instruction and a general immediate data arithmetic instruction;
Fig. 11	is a flowchart illustrative of the operation during the add stack pointer move instruction;
Fig. 12	is a flowchart illustrative of the operation during the subtract stack pointer move instruction;

Fig. 13	is a view illustrative of program execution control during the call and ret instructions;
Fig. 14	shows the bits field of an PC-relative subroutine call instruction;
Fig. 15	is a flowchart illustrative of the operation during the PC-relative subroutine call instruction;
Fig. 16	is a flowchart illustrative of the operation during the ret instruction;
Figs. 17A and 17B	schematically show the actions during the execution of push instructions;
Figs. 18A and 18B	schematically show the actions during the execution of pop instructions;
Fig. 19	shows the bit structure of the pushn and popn instructions;
Fig. 20	is a block diagram of the hardware configuration required for executing the sequential push instruction (pushn) or sequential pop instruction (popn);
Fig. 21	is a flowchart illustrative of the operation during the pushn instruction;
Fig. 22	is a flowchart illustrative of the operation during the popn instruction; and
Fig. 23	is a block diagram of the hardware of a microcomputer in accordance with a second embodiment of this invention.

Description of Preferred Embodiments

[0040] Embodiments of this invention are described below with reference to the accompanying drawings.

Embodiment 1

(1) Configuration of the CPU of this Embodiment

[0041] The CPU of this embodiment executes virtually all of its instructions within one cycle, thanks to its pipeline and load/store architecture. All of the instructions are expressed as 16-bit fixed-length instructions, so that instructions processed by the CPU of this embodiment are implemented within compact object code.

[0042] In particular, this CPU is configured in such a manner that it has a dedicated stack pointer register to enable the efficient coding and execution of processes that act upon the stack pointer. It also enables the decoding and execution of an instruction set of a group of dedicated stack pointer instructions that have object code specifying that dedicated stack pointer register as an implicit operand.

[0043] A schematic view of the circuit structure of the CPU of this embodiment is snown in Fig. 1 by way of illustration.

[0044] This CPU 10 comprises a register set that includes general-purpose registers 11, a PC register 12 for holding the program counter, PSR (processor status register) 13, and a dedicated stack pointer register SP 14; an instruction decoder 20; an immediate data generator 22; an address adder 30; an ALU 40; a PC incrementer 44; various internal buses 72, 74, 76, and 78; and various internal signal lines 82, 84, 86, and 88.

[0045] The instruction decoder 20 decodes object code that has been input, performs the processing necessary for the execution of the resultant instruction, and outputs any necessary control signals. Note that this instruction decoder 20 also functions as a decoding means for decoding the object code of the above mentioned dedicated stack pointer instruction and outputting control signals on the basis of that instruction.

[0046] The immediate data generator 22 generates 32-bit immediate data that will be used during execution, on the basis of immediate data comprised within the object code, and generates the 0, • 1, • 2, and • 4 constant data that is necessary for the execution of each instruction. The PC incrementer 44 updates the program counter stored in the PC 12, on the basis of the execution cycles of the instructions. The address adder 30 adds the data that is stored in the various registers and the immediate data generated by the immediate data generator 22 to generate the address data required during the reading of data from memory. The ALU 40 performs numerical calculations and logical operations.

[0047] This CPU also comprises internal bus and signal lines. The functions of a PA_BUS 72 and a PB_BUS 74 include the transfer of input signals for the ALU 40. The functions of a WW_BUS 76 include the fetching of calculation results from the ALU 40, to transfer them to the general-purpose registers. The functions of an XA_BUS 78 include the transfer of address data that has been fetched from the general-purpose registers 11 and the SP 14. An IA signal line 82 transfers address data from the various components within the CPU to an external I_ADDR_BUS 92. A DA signal line 84 transfers address data from the various components within the CPU to an external D_ADDR_BUS 96. A DIN signal line 86 transfers data from an external D_DATA_BUS 98 to the various components within the CPU. A DOUT signal line 88 transfers data from the various components within the CPU to the external D_DATA_BUS 98. An IA multiplexer 83 switches between signals that are to be output to the IA signal line 82 (signals on the PA_BUS 72, on the WW_BUS 76, from the PC 12, and a value that is the PC plus 2). A DOUT multiplexer 89 switches between signals that are to be output to the DOUT signal line 88 (signals on the PA_BUS 72, on the WW_BUS 76, from the PC 12, and the value that is the PC plus 2).

[0048] Since the components of the CPU 10 execute instructions on the basis of control signals that are output from the instruction decoder 20, they also function as means for executing a group of dedicated stack pointer instructions

on the basis of the above described control signals and the contents of the dedicated stack pointer register.

[0049] This CPU 10 transfers signals to and from the exterior through a 16-bit instruction data bus (I_DATA_BUS) 94, an instruction address bus (I_ADDR_BUS) 92 for instruction data access, the 32-bit data bus (D_DATA_BUS) 98, the data address bus (D_ADDR_BUS) 96 for data access, and a control bus (not shown in the figure) for control signals.

(2) Register Set of the CPU of this Embodiment

[0050] Essential portions of the concept of the register set of the CPU of this embodiment will now be described.

[0051] The register set of the CPU of this embodiment is shown in Fig. 2. This CPU has a register set that comprises the 16 general-purpose registers 11, the PC 12, the PSR 13, the SP 14, ALR (arithmetic low register) 15, and AHR (arithmetic high register) 16.

[0052] The general-purpose registers 11 are functionally equivalent to 32-bit registers and are labeled R0 to R15. These general-purpose registers 11 are used during data calculations and address computations.

[0053] The PC 12 is a 32-bit-long incremental counter that holds a program counter indicating the address of the currently executing instruction. In this document, "PC" is used when referring to the register itself and "program counter" is used when referring to the value stored within the PC.

[0054] The PC- 12 cannot be accessed directly by instructions such as the load instruction. With a call or int instruction, or when an interrupt or exception occurs, the program counter is read from the PC 12 and saved to the stack. In this manner, a jump destination address used when a branch instruction is executed can be set in the PC. This also happens for a branch specified by a conditional branch instruction. The instruction address for the return destination is read from the stack by a ret or reti instruction and is replaced in the PC 12.

[0055] PSR (processor status register) 13 is a 32-bit register to which a flag is allocated, and which holds the current status of the CPU. When an int instruction, an interrupt, an exception, or the like occurs, the state of the PSR at that point is saved to the stack when the flow branches to the corresponding processing routine. Conversely, the execution of the reti instruction causes the saved value to be replaced in the PSR.

[0056] The SP 14 is a 32-bit dedicated stack pointer register containing the stack pointer that indicates the higher address of the stack. In this document, SP is used when referring to the register itself and stack pointer is used when referring to the value stored within the SP. Note, however, that since the stack pointer always points to a word boundary, the lowermost two bits of the stack pointer are always zero.

[0057] This stack pointer is updated at the generation of a trap or at the execution of one of a group of dedicated stack pointer instructions that are provided by this embodiment.

[0058] Examples of these dedicated stack pointer instructions that update the stack pointer include instructions that branch to another routine, sucn as the call and ret instructions, a stack pointer move instruction, a pushn instruction, and a popn instruction. For instance, when the call instruction is executed, the stack pointer is first decremented by an amount equivalent to the word size (-4), then the PC 12 is saved to the stack. Conversely, when the ret instruction is executed, the destination address for return is loaded into the PC from the stack, and the stack pointer is incremented by an amount equivalent to the word size (+4). When an int instruction is executed, or when an interrupt or exception occurs, the value in the PC or PSR is saved to the stack by the following procedure:

1. SP = SP - 4
2. The PC is saved at the higher address of the stack, indicated by the stack pointer.
3. SP = SP - 4
4. The PSR is saved at the higher address of the stack, indicated by the stack pointer.

[0059] When the reti instruction is executed, the above process is reversed to restore the CPU to its original state. Thus the execution of the call, ret, or int instruction causes the stack pointer to be updated as appropriate for that execution. Details of each instruction will be given later.

[0060] A trap function provided by this embodiment comprises interrupts that are generated asynchronously with the execution of instructions and exceptions generated by the execution of instructions. When a trap is generated, the CPU saves PC (program counter) and PSR (process status register) to the stack, then reads a vector table from a trap table and branches to a routine corresponding to that trap. Concomitant with the generation of the trap, IE (interrupt enable) bit is cleared and the generation of subsequent maskable interrupts is inhibited. Maskable external interrupts are enabled again by using a load instruction with respect to the PSR to write 1 to the IE bit.

[0061] The reti instruction is used to return from the trap processing routine to the original routine. When the reti instruction is executed, the CPU reads the PSR and PC from the stack in that order, restores the PSR to its original value and also branches to the return address. Note that exceptions include debugging exceptions, address misalignment exceptions, overflow exceptions, and zero-division exceptions.

[0062] Detailed descriptions of ALR (arithmetic low register) 15 and ALH (arithmetic high register) 16 are omitted.

[0063] The special registers PSR 13, SP 14, ALR 15, and AHR 16 of the CPU are capable of transferring data to and from the general-purpose registers, using load instruction. Each register has a special register number and is accessed by using that number.

Special Register Name	Special Register Number	Assembler Mnemonic
Process status register	0	%PSR
SP	1	%SP
Arithmetic low register	2	%ALR
Arithmetic high register	3	%AHR

(3) Description of Stack and Stack Pointer

[0064] The stack is a temporary storage region provided in memory. It is a contiguous region in which data is written from the bottom up, as if stacked in a rack. The stack pointer indicates the address of the data at the top of the stack, that is, the data that was written most recently into the stack.

[0065] The basic operation of the stack pointer will now be described with reference to Fig. 3.

[0066] Reference number 100 in Fig. 3 denotes a stack region provided in memory. A hatched portion 102 represents data that was most recently stored in this region, and a memory address 1000 indicates that data. Note that a region 104 below the hatched portion 102 contains data that has already been stored and a portion 106 above the hatched portion 102 is available for storing data in the future.

[0067] The stack pointer always indicates a word boundary. This means that, when data is written to the stack, the stack pointer within the SP 14 moves upward by 4 and the data is stored at the location indicated by that stack pointer. When data stored in the stack is fetched, it is the data at the address indicated by the current SP 14 that is fetched and the stack pointer stored in the SP 14 moves downward by 4. In this manner, the stack pointer always indicates the storage address of the data that was stored most recently in the stack.

(4) Description of Group of Dedicated Stack Pointer Instructions

[0068] A RISC CPU always uses a general-purpose register as the stack pointer. This embodiment has the SP 14, which is a dedicated stack pointer register, which is operated upon by the previously mentioned group of dedicated stack pointer instructions.

[0069] This group of dedicated stack pointer instructions is a generic name for a number of instructions that access the SP 14 as an implicit operand and perform operations on the SP 14. The group of dedicated stack pointer instructions comprises instructions that branch to other routines, such as SP-relative load instructions (ld, etc.), stack pointer move instructions (aad, sub), instructions for branching to subroutines (call, etc.), and return instructions (ret, etc.); a sequential push instruction (pushn); and a sequential pop instruction (popn).

[0070] What these instructions have in common is that they are dedicated stack pointer instructions so there is no need for data specifying the stack pointer in the object code. Another common feature is that they enable the efficient coding in short instructions of processes that use the stack pointer.

[0071] The use of these instructions makes it possible to efficiently process data that is stored in a stack provided in memory. Interrupt and subroutine call/return processes can also be performed efficiently.

[0072] An example of the usage of these dedicated stack pointer instructions when a subroutine is called will now be described with reference to Fig. 4. This figure also shows the usage state of the stack provided in memory and the state of the stack pointer. A MAIN program 500 and a subroutine 520 of Fig. 4 are written as object code created by a C compiler. Reference number 540 denotes the state of a stack in memory. Reference number 502 indicates that processing is being performed, using the general-purpose registers R0 to R3. Reference number 506 denotes a subroutine call instruction. Before the subroutine call instruction is executed by the MAIN program 500, in other words, after the previous instruction indicated by 504 has been executed, the stack pointer (SP) points to an address <1> in the stack in memory. When this subroutine call instruction is executed, control passes to the subroutine 520. At this point, an instruction for branching to a subroutine (call instruction), which is one of the dedicated stack pointer instructions of this embodiment, is executed. When this instruction is executed, the value of the stack pointer (SP) is automatically incremented by -4 (at <2> in Fig. 4) and the address for return to the MAIN program is stored in an area 544 of the stack that is indicated by the stack pointer <2>.

[0073] When the subroutine 520 starts executing, it first transfers the values that are stored in the general-purpose registers R0 to R3 used by the MAIN program. Reference number 524 denotes a sequential push instruction (pushn) which is one of the dedicated stack pointer instructions that saves the values stored in the general-purpose registers

R0 to R3 to the stack. When this instruction is executed, the values stored in the general-purpose registers R0 to R3 are transferred in sequence to the stack, so that they are stored in the stack 540 as shown at 550 in Fig. 4. When the execution of this process ends (524 <3>), the stack pointer (SP) is at 546 (<3> SP).

[0074] The subroutine 520 then secures an auto-variable region to be used by the subroutine. An add instruction denoted by 526 is a stack pointer move instruction which is a dedicated stack pointer instruction that causes the stack pointer to move upward to secure a stack region to be used by the subroutine 520. When this instruction is executed, the stack pointer (SP) moves upward by X bytes to a location 548 (<4> SP) to secure an auto-variable region to be used by the subroutine, as stated in Note 2.

[0075] Reference number 528 denotes processing that uses auto-variables and the general-purpose registers R0 to R3 within the subroutine 520. At this point, the location of the stack pointer is as indicated by <5> and the loading of the auto-variables is performed by using a dedicated SP load instruction that is one of the dedicated stack pointer instructions.

[0076] Reference number 529 denotes this SP load instruction that transfers an auto-variable S1 that is stored in memory to the general-purpose register R1. This auto-variable S1 is stored at a location that is offset by Y bytes from the stack pointer (<5> SP). The stack pointer does not move during the above processing of the subroutine 528, so the memory address of the auto-variable is specified by the stack pointer plus the offset. This makes it possible to use the dedicated SP load instruction to fetch data to and from the general-purpose registers efficiently.

[0077] Before control returns from the subroutine 520 to the MAIN program 500, the values in the general-purpose registers R0 to R3 that were saved to the stack must be restored to the general-purpose registers R0 to R3 and the stack pointer must be reset to indicate the area 544 that contains the address for return to the MAIN routine. This restores the stack pointer that was moved by the stack pointer move instruction of 526 back to its original location. A sub instruction indicated by 530 is a stack pointer move instruction which is a dedicated stack pointer instruction that moves the stack pointer downward. When this instruction is executed, the stack pointer moves to 546 (<6> SP). The data 550 stored in the stack is restored to the general-purpose registers R0 to R3. Reference number 532 denotes a sequential pop instruction (popn) which is a dedicated stack pointer instruction that transfers data in the stack to the general-purpose registers R0 to R3. When this instruction is executed, the values 550 stored in the stack are sequentially transferred to the general-purpose registers R0 to R3 so that they are stored in the stack 540 as shown at 550 in Fig. 4. When the execution of this process ends (532 <7>), the stack pointer indicates 544 (<7> SP).

[0078] Reference number 534 denotes a return instruction. When this return instruction is executed control passes to the MAIN program. In this case, a return instruction (ret instruction) which is a dedicated stack pointer instruction is executed by this embodiment. When this instruction is executed, control branches to an instruction that indicates the address for return to the MAIN program, which is stored in the stack area indicated by <7> SP. In other words, the MAIN program 500 returns to the next instruction 507. The value of the stack pointer is automatically incremented by +4 to move it to the top area of the stack used by the MAIN program 500 (<8> SP in Fig. 4).

[0079] The description now turns to details of each of the dedicated stack pointer instructions, as well as the circuit structure required for executing these instructions and the operation during such execution.

(5) Stack Pointer (SP) Relative Load Instructions

[0080] A C compiler creates object code that specifies that an auto-variable region is to be linked to the stack pointer. More specifically, the C compiler acts as means for securing an auto-variable region that is Y bytes long, at an offset of X from the stack pointer.

[0081] A view used for illustrating the process of transferring auto-variables in memory to registers is shown in Fig. 5. In this figure, auto-variable a is word data, auto-variables b and c are each half-word data, and auto-variables d to g are each byte data. The stack pointer stored in the SP indicates 1000, which is the address of the top region of a region 600 of the stack in which auto-variables are stored. An area of the stack at the memory address indicated by the stack pointer is secured as an area for holding the auto-variable a. Areas in the stack at memory addresses indicated by the stack pointer plus 2 and the stack pointer plus 4 are secured as areas for holding the auto-variables b and c, respectively. Similarly, areas in the stack at memory addresses indicated by the stack pointer plus 5, the stack pointer plus 6, the stack pointer plus 7, and the stack pointer plus 8 are secured as areas for holding the auto-variables d to g, respectively. During the execution of a given process, it may be necessary to transfer data between a general-purpose register and an auto-variable which is specified by a memory address that is the stack pointer plus an offset.

[0082] To enable the CPU of this embodiment to execute the above transfer processing efficiently with shorter object code, the following instruction set is provided as SP-relative load instructions that are some of the dedicated stack pointer instructions:

ld.b %Rd, [%sp+imm6] (1)
ld.ub %Rd, [%sp+imm6] (2)

```
ld.h %Rd, [%sp+imm7)     (3)
ld.uh %Rd, [%sp+imm7]    (4)
ld . w %Rd, [%sp+imm8]   (5)
ld.b [%sp+imm6], %Rs     (6)
ld.h [%sp+imm7], %Rs     (7)
ld.w [%sp+imm8], %Rs     (8)
```

Instructions (1) to (8) are instruction codes created by an assembler. Instruction (1) sign-expands byte data and transfers it from the stack to a register, instruction (2) zero-expands byte data and transfers it from the stack to a register, instruction (3) sign-expands half-word data and transfers it from the stack to a register, instruction (4) zero-expands half-word data and transfers it from the stack to a register, instruction (5) transfers word data from the stack to a register, instruction (6) transfers byte data from a register to the stack, instruction (7) transfers half-word data from a register to the stack, and instruction (8) transfers word data from a register to the stack.

[0083] The operands [%sp+imm6], [%sp+imm7], and [%sp+imm8] each represent immediate offset data. A memory address is created by adding an offset that is created during the execution of the instruction on the basis of this immediate offset data and the value of the stack pointer stored in the SP 14. [%sp+imm6] is immediate offset data used when the size of the data in memory is bytes, [%sp+imm7] is that when the data size is half-words, and [%sp+imm8] is that when the data size is words. Whichever size of data is used, it is written as 6-bit immediate offset data 614 in the object code, as will be described later with reference to Fig. 6A. If imm7 is used (in other words, if the data size is half-words), however, the immediate offset data 614 is shifted one bit to the left during the execution of the instruction, to generate an offset to be added to the stack pointer. Similarly, if imm8 is used (in other words, if the data size is words), the immediate offset data 614 is shifted two bits to the left, to generate an offset to be added to the stack pointer.

[0084] In this case, the stack is a temporary storage region provided in memory and the above memory addresses can be used to specify the locations of, for example, auto-variables (a to g) within the stack, as shown in Fig. 5.

[0085] An example of a bit field 610 of these SP-relative load instructions (1) to (8) is shown in Fig. 6A. The SP-relative load instruction of Fig. 6A has 16 bits of object code comprising op code 612 (6 bits) indicating that the operating function is a transfer of data between memory and a general-purpose register, immediate offset data 614 (6 bits) specified by immediate data, and a register number 616 (4 bits) specifying the register that is to be used for the transfer. The op code 612 comprises common code indicating that this is a load instruction that acts upon the SP 14 and different codes specifying each of data size, sign expansion, and zero expansion. Since it is therefore clear from the op code that these instructions act upon the stack pointer stored in the SP 14, there is no necessity to specify data relating to the stack pointer in the operands of the object code. The immediate offset data 614 is used for creating an offset from the stack pointer for data that is to be transferred. This is specified in 6 bits, regardless of the data size, as described above. With instructions (1) to (5), the address (register number) 616 of the register that is involved in the transfer will contain the number of the register to contain data that has been read out from the stack; with instructions (6) to (8), it will contain the number of the register that currently contains data to be written to the stack.

[0086] By way of comparison, Fig. 6B shows an example of a bit field 620 of object code of a load instruction that acts upon a general-purpose register when another general-purpose register is used as the stack pointer (hereinafter called a general-purpose load instruction).

[0087] The general-purpose load instruction of Fig. 6B has 20 bits of object code comprising op code 622 (6 bits) indicating that the operating function is a transfer of data between memory and a general-purpose register, immediate offset data 624 (6 bits) specified by immediate data, a first register number 620 (4 bits) specifying the general-purpose register to be used as the stack pointer, and a second register number 628 (4 bits) specifying the register that is to be used for the transfer. With a general-purpose microcomputer, the instruction length is in 8-bit units, which gives 24-bit or 32-bit instructions.

[0088] Each of Figs. 6A and 6B shows object code for an instruction used when transferring data between a register and a memory address specified by adding an offset to the stack pointer. It is clear from these examples that a SP-relative load instruction can be written with shorter object code than a general-purpose load instruction.

[0089] The description now turns to the configuration required for executing the above instructions and the operations that occur during this execution, taking as examples the instruction (5) that transfers word data from the stack to a register (since this instruction reads word data from the stack to a register, it is hereinafter called an SP-relative load instruction for reading word data) and the instruction (8) that transfers word data from a register to the stack (since this instruction writes word data from a register to the stack, it is hereinafter called an SP-relative load instruction for writing word data).

[0090] The hardware configuration necessary for executing the instructions will be described first, using Fig. 1 for reference. Each of these instructions is transferred over the I_DATA_BUS 94 from an external memory (ROM) 52 and is input to the instruction decoder 20. The instruction is decoded by the instruction decoder 20, which outputs various signals (not shown in the figure) necessary for executing the instruction. The immediate data generator 22 performs

a leftward logical shift on the immediate offset data 614 in accordance with the data size, generates the offset used during the execution of sign expansion or zero expansion, if necessary, and outputs the results to the PB_BUS 74. The SP 14 contains the stack pointer, and that value can be output to the XA_BUS 78 which is connected to an input of the address adder 30. Another input of the address adder 30 is connected to the PB_BUS 74 that is an output of the immediate data generator 22. An output (ADDR) of the address adder 30 is connected to the external D_ADDR_BUS 96 by the DA signal line 84.

[0091] BCU (bus control unit) 60 controls the input and output of data to and from memory (RAM and ROM) 50 and 52 (which includes the stack area) and outputs READ and WRITE control signals in accordance with various request signals that are output from the CPU (such as signals output to external buses).

[0092] The description first concerns the operation during the execution of an SP-relative load instruction for reading word data.

[0093] When the SP-relative load instruction for reading word data is executed, the value of the stack pointer stored in the SP 14 is added to the offset created by the immediate data generator 22 on the basis of the immediate offset data 614, to create a memory address for reading. Data is read from memory on the basis of this memory address and is transferred to the general-purpose register specified by the register number 616 in the object code.

[0094] A flowchart illustrating the operation during the SP-relative load instruction for reading word data is shown in Fig. 7.

[0095] At the start of execution of this instruction, the stack pointer stored in the SP 14 is output to the XA_BUS 78 (step S210). An offset imm created by the immediate data generator 22 from the immediate offset data is then output to the PB_BUS 74 (step S212). The address adder 30 adds the value on the XA_BUS 78 and the value on the PB_BUS 74, then outputs the resultant memory read address (ADDR) over the DA signal line 84 to the D_ADDR_BUS 96 (steps S214 and S216). A data read request signal from the CPU to the BCU 60 becomes active and executes an external memory read cycle (step S218). In other words, the BCU 60 follows the request signal to control the reading of data from memory, using this read address as a memory address, and the output of the data to the D_DATA_BUS 98. The data on the D_DATA_BUS 98 is output to the WW_BUS 76 over the DIN signal line 86 (step S220). The value on the WW_BUS 76 is stored in the register (%Rd) having the register number specified by the 4-bit address 616 of the register (Ra/Rs) that is specified in the instruction code for the transfer (step S222).

[0096] The description now turns to the operation during the execution of an SP-relative load instruction for writing word data

[0097] When the SP-relative load instruction for writing word data is executed, the value of the stack pointer stored in the SP 14 is added to the offset created by the immediate data generator 22 on the basis of the immediate offset data 614, to create a memory address for writing to memory. The data stored in the general-purpose register specified by the register number 616 in the object code is transferred to the areas in memory specified by that memory address.

[0098] A flowchart illustrating the operation during the SP-relative load instruction for writing word data is shown in Fig. 8.

[0099] At the start of execution of this instruction, the stack pointer stored in the SP 14 is output to the XA_BUS 78 (step S230). An offset imm created by the immediate data generator 22 from the immediate offset data is then output to the PB_BUS 74 (step S232). The address adder 30 adds the value on the XA_BUS 78 and the value on the PB_BUS 74, then outputs the resultant memory write address (ADDR) over the DA signal line 84 to the D_ADDR_BUS 96 (steps S234 and S236). The data stored in the register (%Rd) having the register number specified by the 4-bit address 616 of the register (Rs/Rd) that is specified in the instruction code for the transfer is output to the PA_BUS 72 (step S238). The data on the PA_BUS 72 is output to the D_DATA_BUS 98 over the DOUT signal line 88 (step S240). A data write request signal from the CPU to the BCU 60 becomes active and executes an external memory write cycle (step S242). In other words, the BCU 60 follows the request signal to control the operation of writing to memory the data that has been transferred to the D_DATA_BUS 98, using this write address as a memory address.

(6) Stack Pointer Move Instruction

[0100] Views used to illustrate the usage state of the stack in memory and the state of the stack pointer during each routine of a program that extends over a plurality of routines are shown in Figs. 9A to 9F.

[0101] The states of the stack region in memory and the stack pointer. (the value stored in the SP 14) during the execution of a given process 'a' 211 of a MAIN routine 210 of Fig. 9A are shown in Fig. 9D. Reference number 222 denotes a stack region that is to be used by the MAIN routine 210, and the stack pointer indicates a higher address 232 of the region 222

[0102] A SUB1 routine 212 of Fig. 9B is a subroutine that is called and executed from the MAIN routine 210. The states of the stack region in memory and the stack pointer (the value stored in the SP 14) during the execution of a given process 'b' 213 of the SUB1 routine 212 are shown in Fig. 9E. Reference number 224 denotes a stack regicn that is to be used by the SUB1 routine 212, and the stack pointer indicates a higher address 234 of the region 224.

[0103] A SUB2 routine 214 shown in Fig. 9C is called ano executed from the SUB1 routine 212. The states of the stack region in memory and the stack pointer (the value stored in the SP 14) during the execution of a given process 'c' 215 of the SUB2 routine 214 are shown in Fig. 9F. Reference number 226 denotes a stack region that is to be used by the SUB2 routine 214, and the stack pointer indicates a higher address 236 of the region 226.

[0104] When execution extends over a plurality of subroutines in this manner, the stack region used by each routine moves, so that the value of the stack pointer is moved as appropriate to the top of the stack region used by each routine.

[0105] To enable the CPU of this embodiment to execute this movement of the stack pointer efficiently with shorter object code, the following instruction set is provided as stack pointer move instructions that are some of the dedicated stack pointer instructions:

```
add %sp,imm12    (9)
sub %sp, imm12   (10)
```

Instructions (9) and (10) are instruction codes created by an assembler. Instruction (9) is an immediate data add instruction for the stack pointer stored in the SP 14 and instruction (10) is an immediate data subtract instruction for this stack pointer. The operand imm12 is 32-bit data obtained by shifting the 10-bit immediate data by two bits leftward then subjecting it to zero expansion. It is used for ooerations with the stack pointer that is stored in the SP 14.

[0106] A bit field 630 of the stack pointer move instructions (9) and (10) is shown in Fig. 10A. The stack pointer move instruction of Fig. 10A has 16 bits of object code comprising op code 632 (6 bits) indicating whether the move data for the stack pointer stored in the SP 14 is an addition or subtraction and immediate data 634 (10 bits). This op code 632 comprises common code indicating that this is a stack pointer move instruction that acts upon the SP 14 and different codes specifying either addition or subtraction. Since it is therefore clear from the op code that these instructions operated upon the stack pointer stored in tne SP 14, there is no necessity to specify data relating to the stack pointer in the operands of the object code. The immediate offset data 634 is used for creating an offset for subtracting from or adding to the stack pointer.

[0107] By way of comparison, Fig. 10B shows an example of a bit field 640 of object code of an add/subtract instruction when a general-purpose register is used as the stack pointer, (hereinafter called a general-purpose calculation instruction).

[0108] The general-purpose calculation instruction of Fig. 10B has 20 bits of object code comprising op code 642 (6 bits) indicating that the operating function is a addition or subtraction of immediate data to or from a value in a general-purpose register, immediate data 644 (10 bits), and a register number 646 (4 bits) specifying the register that is to be operated upon. with a general-purpose microcomputer, the instruction length is in 8-bit units, which gives 24-bit or 32-bit instructions.

[0109] Each of Figs. 10A and 10B shows object code for an instruction used when adding or subtracting immediate data to or from the stack pointer. It is clear from these examples that a stack pointer move instruction can be written with shorter object code than a general-purpose calculation instruction.

[0110] The description now turns to the configuration required for executing me above instructions and the operations that occur during this execution, taking as an example the instruction (9) that adds immediate data to the SP (hereinafter called an add stack pointer move instruction) and the instruction (10) that subtracts immediate data from the SP (hereinafter called a subtract stack pointer move instruction).

[0111] The hardware configuration necessary for executing the instructions will be described first, using Fig. 1 for reference. Each of these instructions is transferred over the I_DATA_BUS 94 from an external memory (ROM) 52 and is input to the instruction decoder 20. The instruction is decoded by the instruction decoder 20, which outputs various signals (not shown in the figure) necessary for executing the instruction. The immediate data generator 22 performs a logical shift by two bits to the left on the 10 bits of the immediate data 634, subjects it to zero expansion, and outputs it to the PA_BUS 72. The SP 14 contains the stack pointer, and that value is output to the XA_BUS 78. The XA_BUS 78 is connected to the PB_BUS 74 which forms an input of the ALU 40. Another input of the ALU 40 is connected to the PA_BUS 72 that is an output of the immediate data generator 22. The outout of the ALU 40 is connected to the WW_BUS 76. This WW_BUS 76 is connected to the input of the SP.

[0112] The description first concerns The operation during the execution of the add stack pointer move instruction.

[0113] When the add stack pointer move instruction is executed, the value of the stack pointer stored in the SP 14 is added to the offset created by the immediate data generator 22 on the basis of the immediate offset data 634, to create a new stack pointer. That value is stored in the SP 14.

[0114] A flowchart illustrating the operation during the add stack pointer move instruction is shown in Fig. 11.

[0115] At the start of execution of this instruction, the stack pointer stored in the SP 14 is output to the XA_BUS 78 (step S250). The data on the XA_BUS 78 is output to the PB_BUS 74 (step S252). Move immediate data imm created by the immediate data generator 22 on the basis of the immediate data is output to the PA_BUS 72 (step S254). The ALU 40 adds the value on the PB_BUS 74 and the value on the PA_BUS 72, and outputs the result to the WW_BUS

76 (step S256). The value on the WW_BUS 76 is then input to the SP 14 (step S258). The description now turns to the operation during the execution of the subtract stack pointer move instruction.

[0116] When the subtract stack pointer move instruction is executed, the move immediate data created by the immediate data generator 22 on the basis of the immediate data 634 is subtracted from the value of the stack pointer stored in the SP 14 to create a new stack pointer. That value is stored in the SP 14.

[0117] A flowchart illustrating the operation during the subtract stack pointer move instruction is shown in Fig. 12.

[0118] At the start of execution of this instruction, the stack pointer stored in The SP 14 is output to the XA_BUS 78 (step S260). The data on the XA_BUS 78 is then output to the PB_BUS 74 (step S262). Move immediate data imm created by the immediate data generator 22 on the basis of the immediate data is output to tne PA_BUS 72 (step S264). The ALU 40 subtracts the value on the PA_BUS 72 from the value on the PB_BUS 74, and outputs the result to the WW_BUS 76 (step S266). The value on the WW_BUS 76 is then input to the SP 14 (step S268).

(7) Branch Instruction

[0119] A view illustrating program execution control during the call and ret instructions is shown in Fig. 13. During a MAIN routine 300 shown in Fig. 13, a call instruction (302) is executed to branch to a subroutine SUB 310, so that control passes to the subroutine SUB 310. A ret instruction (312) is placed at the end of the subroutine. When this instruction is executed, the flow returns to the next the instruction (304) after the call instruction (302) of the MAIN routine 300. Therefore, the program is executed in the sequence <1>, <2>, then <3> in Fig. 13. At the end of the execution of this subroutine SUB 310, control returns to the MAIN routine 300 and execution is to continue from the next instruction (304) after the call instruction (302). This makes it necessary to record the address of the return destination somewhere, when a branch occurs to the subroutine SUB 310. For that reason, the return destination address is saved to the stack as shown in Fig. 4 during tne execution of a branch instruction that branches to a subroutine, sucn as the call instruction, then the return destination address is returned from the stack to the program counter during the execution of a branch instruction that returns frcm a subroutine, such as the ret instruction (this process is hereinafter called saving and restoring the program counter).

[0120] With a prior-art RISC CPU, the process of saving and restoring the program counter is dcne by software, so that it is necessary to provide object code (assembler instructions) for executing this process during the execution of a branch instruction such as the call instruction. For example, it is necessary to provide object code (assembler instructions) for decrementing tne stack pointer by an amount equivalent to the word size (4) during the execution of the call instruction, to place the address of the next instruction after the call instruction in the stack on the basis of the value in the program counter.

[0121] The CPU of this embodiment, however, has a hardware configuration that enables the saving and restoration of the program counter when the call or ret instruction is executed. It is therefore not necessary to provide object code (assembler instructions) that saves and restores the program counter separately from the object code of the call and ret instructions.

[0122] To enable the CPU of this embodiment to execute this process of saving and restoring the program counter by a single instruction, the following instruction set is provided as branch instructions that are some of the dedicated stack pointer instructions:

call sign9	(11)
call %Rb	(12)
ret	(13)
reti	(14)
retd	(15)
int imm2	(16)
brk	(17)

Instructions (11) to (17) are instruction codes created by an assembler. Instruction (11) is a PC-relative subroutine call instruction which uses the program counter (PC) as a base address, to branch in a relative manner to a branch destination address on the basis of the displacement data sign9 specified as the operand. Instruction (12) is a register indirect subroutine call instruction which branches to the branch destination address contained within the register specified as the operand. Instruction (13) is an instruction for return from a subroutine. Instruction (14) is an instruction for return from an interrupt or exception processing routine. Instruction (15) is an instruction for return from a debugging processing routine. Instruction (16) is a software interrupt instruction. Instruction (17) is a software/debugging interrupt instruction.

[0123] An example of a bit field 650 of the PC-relative subroutine call instruction (11) is shown in Fig. 14. The PC-relative subroutine call instruction of Fig. 14 has 16 bits of object code comprising op code 652 (8 bits) indicating that

the operating function is a call instruction that branches to a subroutine with a branch destination address that is specified relatively, using the program counter as a base address, and displacement data sign9 (8 bits) 654 specified by immediate data. During the execution of this command, the 8-bit immediate data is shifted logically by one bit to the left then is subjected to sign expansion.

[0124] The CPU of this embodiment is capable of saving the program counter to the stack at the execution of the call instruction, with only the object code shown in Fig. 14.

[0125] The description now turns to the configuration required for executing the above instructions and the operations that occur during this execution, taking as examples the PC-relative subroutine call instruction (11) as an instruction for branching to a subroutine and the return instruction (13) as an instruction for returning from the subroutine.

[0126] The hardware configuration necessary for executing the instructions will be described first, using Fig. 1 for reference. Each of these instructions is transferred over the I_DATA_BUS 94 from external memory (ROM) 52 and is input to the instruction decoder 20. The instruction is decoded by the instruction decoder 20, which outputs various signals (not shown in the figure) necessary for executing the instruction. The immediate data generator 22 performs a logical shift by one bit to the left on the displacement data 654, subjects it to sign expansion to create a 32-bit immediate data displace-ment imm, then outputs the result to the PB_BUS 74. The SP 14 contains the stack pointer, and that value is output to the XA_BUS 78 which is connected to an input of the address adder 30. Another input of the address adder 30 is connected to the PB_BUS 74 that is an output of the immediate data generator 22. An output (ADDR) of the address adder 30 is connected to the external I_ADDR_BUS 92 by the IA signal line 82.

[0127] The I_ADDR_BUS 92 and I_DATA_BUS 94 are connected to the ROM 52 in which is stored the instruction object code. The bus control unit (BCU) 60 outputs READ control signals that read this instruction object code from the memory (ROM) 52 in accordance with various request signals that are output from the CPU (such as signals output to external buses).

[0128] The description first concerns the operation during the execution of an PC-relative subroutine call instruction.

[0129] When the PC-relative subroutine call instruction is executed, the value of the program counter stored in the PC 12 is saved to the stack as described with reference to Fig. 4, and the value of the stack pointer stored in the SP 14 is decremented by the word size (4). A branch destination address obtained by adding the program counter and the 32-bit immediate data displacement is set in the PC 12.

[0130] A flowchart illustrating the operation during the PC-relative subroutine call instruction is shown in Fig. 15.

[0131] At the start of execution of this instruction, the stack pointer stored in the SP 14 is output to the XA_BUS 78 (step S270). This forms one input of the address adder, and constant data (-4) created by the immediate data generator 22 forms the other input of the address adder 30. The constant -4 is added to the value of the stack pointer on the XA_BUS 78 by the address adder 30 to create a write address to the stack for storing the return address, and the result is output to the WW_BUS 76. This write address is output to the D_ADDR_BUS 96 (step S272). The value of the program counter stored in the PC 12 is incremented by 2 by the PC incrementer 44 to create the return address, and the result is output to the D_DATA_BUS 98 over the DOUT signal line 88 (steo S274) . A data write request signal from the CPU to the BCU 60 becomes active and executes an external memory write cycle (step S276). In other words, the BCU 60 follows the request signal to store this return address in tne stack provided in memory, using this write address as a memory address.

[0132] The value on the WW_BUS 76 is then output to the SP 14 (step S278). In other words, the value of the stack pointer is updated by being decremented by 4.

[0133] The program counter stored in the PC 12 is then output to the XA_BUS 78 (step S280). The immediate data generator 22 performs a logical shift by one bit to the left on the displacement data 654, subjects it to sign expansion to create a 32-bit immediate data displacement imm, then outputs the result to the PB_BUS 74. The address adder 30 adds the program counter on the XA_BUS 78 and the immediate data displacement imm on the PB_BUS 74 to create a branch address (ADDR), then outputs that address over the IA signal line 82 to the I_ADDR_BUS 92 (step S282). An instruction read request signal from the CPU to the BCU 60 becomes active and executes a read cycle with respect to the external memory (ROM) 52 to fetch the object code of the branch destination instruction (step S284).

[0134] The operation during the execution of the ret instruction will now be described.

[0135] When the ret instruction is executed, the value of the program counter that was saved to the stack is restored to the PC 12, and the value of the stack pointer stored in the SP 14 is incremented by the word size (4), as described with reference to Fig. 4.

[0136] A flowchart illustrating the operation during the ret instruction is shown in Fig. 16.

[0137] Before this instruction is executed, the stack pointer stored in the SP 14 indicates the address in the stack containing the destination address for return from the called routine.

[0138] At the start of execution of this instruction, the stack pointer stored in the SP 14 is output to the XA_BUS 78 (step S290). The stack pointer on the XA_BUS 78 is then output to the D_ADDR_BUS 96 (step S292). A data read request signal from the CPU to the BCU 60 becomes active and executes an external memory read cycle. In other words, the BCU 60 follows the request signal to read the return address from the stack provided in memory, using the

stack pointer as a memory address. This return destination address that has been read from the memory (RAM) 50 is fetched within the CPU from the D_DATA_BUS 94 over the DIN signal line 86, then is output from the DIN signal line 86 to the I_ADDR_BUS 92 over the IA signal line 82 (step S294). An instruction read request signal from the CPU to the BCU 60 becomes active and executes a read cycle with respect to the external memory (ROM) 52 to fetch the object code of the return destination instruction (step S296).

[0139] The value of the stack pointer on the XA_BUS 78 is one input of the address adder 30, and constant data (+4) created by the immediate data generator 22 forms the other input of the address adder 30. The constant +4 is added to the value of the stack pointer on the XA_BUS 78 by the address adder 30 to create the address of the top area of the stack region secured by the return destination routine, and the result is output to the WW_BUS 76 (step S298). This address on the WW_BUS 76 (the address of the top area of the stack region secured by the return destination routine) is then output to the SP 14 (step S300).

(8) Description of Sequential Push Instruction (pushn) and Sequential Pop Instruction (popn)

[0140] As described previously, it has recently become common to have a configuration with a large number of internal general-purpose registers, particularly in RISC CPUs, to enable processes to run rapidly within the CPU itself, without having to access memory. The CPU of this embodiment incorporates 16 general-purpose registers, designed to increase the speed of processing. However, if there are so many internal registers, the contents of a large number of registers have to be saved during processing that saves and restores registers when an interrupt occurs or a subroutine is called.

[0141] When the contents of these registers are saved or restored in the prior art, a push instruction for storing the contents specified by an address or a pop instruction for fetching the contents of the stack to a register is used. The actions of these ordinary push and pop instructions will now be described.

[0142] The actions performed during the execution of push instructions are shown schematically in Figs. 17A and 17B and the actions during the execution of pop instructions are shown schematically in Figs. 18A and 18B. The actions performed when data is transferred between a plurality of general-purpose registers and the stack will now be described, with reference to Figs. 17A, 17B, 18A, and 18B.

[0143] Fig. 17A shows the actions when a 'push R1' instruction is executed, to write the contents of a general-purpose register R1 to the stack. During the execution of this instruction, the contents of the SP 14 are updated by the subtraction of 4 from the current value (1000 in Fig. 17A is updated to 996). The contents 'a' of the general-purpose register R1 are written to 996, which is the memory address indicated by the updated stack pointer in the SP 14.

[0144] Fig. 17B shows the actions when a 'push R2' instruction is executed to further write the contents of a general-purpose register R2 to the stack. During the execution of this instruction, the contents of the SP 14 are updated by the subtraction of 4 from the current value (996 in Fig. 17B is updated to 992). The contents 'b' of the general-purpose register R2 are written to 992, which is the memory address indicated by the updated stack pointer in the SP 14.

[0145] Fig. 18A shows the actions when a 'pop R2' instruction is executed to fetch the contents of the stack to the general-purpose register R2. During the execution of this instruction, the contents 'b' stored at the memory address 992 indicated by the stack pointer in the SP 14 are fetched and stored in the general-purpose register R2. The contents of the SP 14 are updated by the addition of 4 to the current value (the pre-execution value of 992 in Fig. 18A is updated to 996).

[0146] Finally, Fig. 18B shows the actions when a 'pop R1' is executed to further fetch the contents of the stack to the general-purpose register R1. During the execution of this instruction, the contents 'a' stored at the memory address 996 indicated by the stack pointer in The SP 14 are fetched and stored in the general-purpose register R1. The contents of the SP 14 are updated by the addition of 4 to the current value (the pre-execution value of 996 in Fig. 18B is updated to 1000).

[0147] When data is transferred between a plurality of general-purpose registers and tne stack in this example of the prior art, it is necessary to execute push or pop instructions a plurality of times. This is because each execution of a push or pop instruction can only operate on a single register.

[0148] Therefore, when processing is performed to save data from a number of registers to the stack, or recover data from the stack to a number of registers, the resultant increase in the number of instructions will lead toan increase in the size of the object code. The number of execution steps in the program will also increase, leading to delays in the execution time or processing of the program.

[0149] The following instruction set is provided for the CPU of this embodiment:

pushn %Rs (18)
popn %Rd (19)

Instruction (18) is a sequentialoush instruction created by an assembler. It sequentially pushes the contents of n gen-

eral-purpose registers (where n is an integer from 1 to 16) from %Rs to R0 onto the stack. Instruction (19) is a sequential pop instruction created by an assembler. It sequentially pops n items of word data (where n is an integer from 1 to 16) from the stack and pushes them into general-purpose registers %Rd to R0. Each of the pushn and popn instructions consists of op code and an operand. The operand %Rs of the pushn instruction indicates the register number of Rs when data is to be written to the stack from registers %Rs to R0. The operand %Rd of the popn instruction indicates the register number of Rd when data is to be taken from the stack and written to registers R0 to %Rd.

[0150] The bit structure of the pushn and popn instructions is shown in Fig. 19. The lowermost 4-bit field contains a code indicating %Rs or %Rd; any of the 16 general-purpose registers can be specified. When data is to be transferred between a special register and the stack, it is transferred via a general-purpose register.

[0151] A block diagram of the hardware configuration required for executing the sequential push instruction (pushn) or sequential pop instruction (popn) is shown in Fig. 20. Portions necessary for the description of the sequential push instruction (pushn) and sequential pop instruction (popn) are extracted from Fig. 1, and further necessary portions are added. Portions that are the same as those in Fig. 1 are given the same reference numbers. In this figure, reference number 11 denotes 16 general-purpose registers called R0 to R15. These general-purpose registers 11 transfer data to and from the D_DATA_BUS 98. A register selection address signal 54 for selecting a register comes from a control circuit block 45. The stack pointer is stored in the SP 14. The value in the SP 14 can be output to the D_ADDR_BUS 96 and the internal address bus (XA_BUS) 78 that is connected to an input of the 32-bit address adder 30. Another input of the address adder 30 is connected to an offset signal 24 that is output from the control circuit block 45. An output of the address adder 30 is held by a latch (Add_LT) 32, then is further output to the XA_BUS 78 or tne WW_BUS 76. The WW_BUS 76 is connected to the input of the SP 14. There is a 4-bit counter (countx) 46 in the control circuit block 45, to count the number of registers involved in the data transfer. The control circuit block 45 is further provided with an instruction register (not shown in the figure), which holds the operand %Rs or %Rd of the pushn or popn instruction and also outputs control signals in accordance with instructions from the instruction decoder. In this figure, reference number 60 denotes a bus control unit (BCU) that controls the input and output of data to and from external memory (RAM) 50, which includes the stack area and outputs READ and WRITE control signals.

[0152] The description first concerns the operation during the execution of a sequential push instruction (pushn).

[0153] When the sequential push instruction (pushn) is executed, the contents stored in the general-purpose registers are sequentially pushed into the stack, starting with the register with register number %Rs to general-purpose register R0, as described previously with reference to Fig. 4.

[0154] A flowchart illustrating the operation during the pushn instruction is given in Fig. 21.

[0155] At the start of execution of the pushn instruction, the offset of a offset signal 24 is -4. The counter (countx) 46 is cleared to zero and the stack pointer stored in the SP 14 is output to the XA_BUS 78 (step S100).

[0156] The address adder 30 then adds -4 to the value on the XA_BUS 78 and inputs the result to the latch (Add_LT) 32 (step S101).

[0157] The value in the latch (Add_LT) 32 is then output to the D_ADDR_BUS 96. The difference between the value of %Rs held in the lowermost 4 bits of the instruction register and the value in counter (countx) 46 is calculated by the control circuit block 45 and output tc the register selection address signal 54. The register selected by this signal 54 is linked to the D_DATA_BUS 98 and a write is performed with respect to the external memory (RAM) 50 (step S102).

[0158] In a step S103, the counter (countx) 46 is compared with %Rs. If they match, the writing of registers to external memory has been completed and the execution of the pushn instruction ends by the writing of the value in the latch (Add_LT) 32 to the SP 14 through the WW_BUS 76 (step S104).

[0159] If they do not match, the counter (countx) is incremented by 1, the value in the latch (Add_LT) 32 is output to the XA_BUS 78, and the processing from step S101 onward is repeated (step S105).

[0160] The operation during the execution of a sequential pop instruction (popn) will next be described.

[0161] When a sequential pop instruction (popn) is executed, the contents of the stack are sequentially pushed from the general-purpose register R0 to the general-purpose register with register number %Rd, as described above with reference to Fig. 4.

[0162] A flowchart illustrating the operation during the popn instruction is shown in Fig. 22.

[0163] At the start of execution of the popn instruction, the offset of a offset signal 24 is +4. The counter (countx) 46 is cleared to zero and the stack pointer stored in the SP 14 is output to the XA_BUS 78 and the D_ADDR_BUS 96 (step S110).

[0164] The address adder 30 then adds 4 to the value in the XA_BUS 78 and inputs the result to the latch (Add_LT) 32 (step S111).

[0165] An external memory read cycle is then performed. The thus-read data is written to the general-purpose registers 11 through the D_DATA_BUS 98. During this time, the counter (countx) 46 is output to the register selection address signal 54 by the control circuit block 45 (step S112).

[0166] In a step S113, the counter (countx) 46 is compared with %Rs. If they match, the reading from external memory to registers has been completed and the execution of the popn instruction ends by the writing of the value in the latch

(Add_LT) 32 to the SP 14 through the WW_BUS 76 (step S114).

[0167] If they do not match, the counter (countx) is incremented by 1, the value in the latch (Add_LT) 32 is output to the XA_BUS 78 and the D_ADDR_BUS 96, and the processing from step S111 onward is repeated (step S115).

[0168] Thus the 'pushn %Rs' instruction makes it possible to write data from registers %Rs to R0 to the stack and the 'popn %Rd' instruction makes it possible to return the necessary number of data items from the stack to registers R0 to %Rd. Thus data from registers R3 to R0 can be pushed by the execution of 'pushn %Rs', for example.

[0169] A further increase in efficiency is achieved in this case by the addition of a restriction over the way in which registers are used. In other words, the saving and restoration of register is particularly necessary when a program branches to another routine, such as during interrupt processing or when a subroutine is called. It is preferable that each routine called in such a case, such as another interrupt routine or subroutine, uses the registers in sequence from R0. This ensures that the contents of registers can be efficiently saved or restored by using the pushn instruction or popn instruction, without having to include registers from R0 to Rd or Rs that contain data that does not need to be saved. All of the registers in this embodiment have the same functions, and there are no other restrictions on the usage of registers and the instruction, so that this restriction solves the above problem without causing further problems.

[0170] Therefore, use of the pushn instruction and popn instruction of this embodiment makes it possible to implement efficient saving of data from registers to the stack in memory and the restoration of data from the stack to registers by a single instruction of either pushn or popn. This minimizes the object code size and the number of program execution steps, and also means that the number of execution cycles can be reduced to a single instruction fetch and the necessary number of data transfers, enabling a minimization of the number of cycles. This makes it possible to increase the speed of interrupt processing routines and subroutines.

[0171] Since the structural elements required for this execution are a count means and a simple sequence controller, it is possible to implement a data processing circuit with a small number of gates so that this invention can be applied to a one-chip microcomputer.

[0172] The above description concerned the configuration required for executing the sequential push instruction (pushn) and sequential pop instruction (popn) when a dedicated stack pointer register is used as the SP 14, but it should be obvious to those skilled in the art that the present invention can also be applied to a structure in which any general-purpose register is used as tne stack pointer.

Embodiment 2

[0173] A block diagram of the hardware of a microcomputer in accordance with this embodiment is shown in Fig. 23.

[0174] This microcomputer 2 is a 32-bit microcontroller that comprises a CPU 10; ROM 52; RAM 50; a high-frequency oscillation circuit 910; a low-frequency oscillation circuit 920; a reset circuit 930; a prescaler 940; a 16-bit programmable timer 950; a 8-bit programmable timer 960; a clock timer 970; an intelligent DMA 980; a high-speed DMA 990; an interrupt controller 800; a serial interface 810; a bus control unit (BCU) 60; an A/D converter 830; a D/A converter 840; an input port 850; an output port 860; and an I/O port 870; as well as various buses 92, 94, 96, and 98 that are connected to these components and various pins 890.

[0175] The CPU 10 has an SP that is a dedicated stack pointer register, and it decodes and executes the dedicated stack pointer instructions as described above. This CPU 10 has the same configuration as that of the previously described Embodiment 1 and it functions as a decoding means and execution means.

[0176] The microcomputer of this embodiment can therefore enable efficient coding and execution of processes that act upon the stack pointer, with short instructions.

[0177] The processes of saving and restoring registers can also be coded efficiently, so that interrupt processing and subroutine call/return can be performed rapidly.

[0178] The microcomputer of this invention can be applied to peripheral equipment for personal computers, such as printers, or electronic equipment such as portable appliances, for example. Such applications of the invention make it possible to provide inexpensive, but sophisticated, electronic equipment that is facilitated by a data processing circuit that has a fast processing speed and a highly efficient usage of memory.

[0179] Note that this invention is not to be taken as being limited to the above described embodiments; it can be embodied in various other ways.

Claims

1. A data processing circuit comprising:

   a dedicated stack pointer register that is used only for the stack pointer (14);
   decoding means (20) for decoding object code of a group of dedicated stack pointer instructions which have

object code specifying said dedicated stack pointer register as an implicit operand and which relate to processing based on said dedicated stack pointer register, and for outputting a control signal based on said object code, execution means (10) for executing said group of dedicated stack pointer instructions based on said control signal and the contents of said dedicated stack pointer register; and
a plurality of registers (11) provided in a contiguous sequence, wherein said group of dedicated stack pointer instructions comprises at least one of a sequential push instruction and a sequential pop instruction having data for specifying a plurality of registers in the object code thereof;

said decoding means (20) decodes at least one of said sequential push instruction and said sequential pop instruction; and
said execution means (10) performs at least one of a process of executing a plurality of sequential pushes of data from said plurality of registers to a stack provided in memory and a process of executing a plurality of sequential pops of data from said stack to said plurality of registers, based on the contents of a memory address specified by said dedicated stack pointer register (14) and said data for specifying a plurality of registers, during the execution of at least one of said sequential push instruction and said sequential pop instruction;
characterized in that
said execution means (10) comprises:

write means for writing the contents of a given register that is one of said plurality of registers (11) to a stack provided in memory (50B), based on a memory address specified by said dedicated stack pointer register (14);
number-of-times-written count means (46) for counting the number-of-times-written of said write means; and
comparison means (45) for comparing said number-of-times-written counted by said count means with the value of said data for specifying a plurality of registers;

wherein said write means comprises:

write memory address generation means (30, 32) for adding a first input and a second input by an adder, and for generating a write memory address for specifying a write destination:
first input control means (45) for providing control such that the first input of said adder is the contents of said dedicated stack pointer register at the start of execution of a sequential dedicated instruction, and is a write address generated subsequently by a write address generation means;
second input control means (45) for outputting an offset used during the writing of one word to said stack to the second input of said adder; and
write means (45) for writing to said stack the contents of a register specified by subtraction processing which uses said data for specifying a plurality of registers and said number-of times-written, based on said write memory address;

whereby the writing of the contents of said plurality of registers to said stack and the ending of said writing are controlled based on the comparison result of said comparison means.

2. A data processing circuit comprising:

a dedicated stack pointer register that is used only for the stack pointer (14);
decoding means (20) for decoding object code of a group of dedicated stack pointer instructions which have object code specifying said dedicated stack pointer register as an implicit operand and which relate to processing based on said dedicated stack pointer register, and for outputting a control signal based on said object code;
execution means (10) for executing said group of dedicated stack pointer instructions based on said control signal and the contents of said dedicated stack pointer register; and
a plurality of registers (11) provided in a contiguous sequence,

wherein said group of dedicated stack pointer instructions comprises at least one of a sequential push instruction and a sequential pop instruction having data for specifying a plurality of registers in the object code thereof;
said decoding means (20) decodes at least one of said sequential push instruction and said sequential pop instruction; and
said execution means (10) performs at least one of a process of executing a plurality of sequential pushes of data from said plurality of registers to a stack provided in memory and a process of executing a plurality of sequential pops of data from said stack to said plurality of registers, based on the contents of a memory address specified by said dedicated stack pointer register (14) and said data for specifying a plurality of registers, during

the execution of at least one of
characterized in that
said execution means (10) comprises:

read means for reading the contents of a stack provided in memory based on a memory address specified by said dedicated stack pointer register, and storing said contents in a given register of said plurality of registers;
number-of-times-read count means for counting the number-of-times-read of said read means; and
comparison means (45) for comparing said number-of-times-read counted by said count means with the value of said data for specifying a plurality of registers;

wherein said read means comprises:

first input control means (45) for providing control such that the first input of an adder is the contents of said dedicated stack pointer register at the start of execution of a sequential dedicated instruction, and is a read memory address generated subsequently by a read address generation means;
second input control means (45) for outputting an offset used during the reading of one word from said stack to the second input of said adder;
read means (45) for reading the contents of said stack based on said read memory address and storing said contents in a register specified based on said number-of-times-read;

whereby the reading of the contents of said stack and the ending of said reading are controlled based on the comparison result of said comparison means.

3. The data processing circuit as defined in claim 1 or 2, further comprising:

n general-purpose registers (11) specified by register numbers 0 to n-1;

wherein object code of at least one of said sequential push instruction and said sequential pop instruction comprises a final register number to which one of said register numbers is specified, as said data for specifying a plurality of registers; and
said execution means (10) performs at least one of a process of executing a plurality of sequential pushes of data into a stack provided in memory from a plurality of registers starting from register 0 to a register specified by said final register number and a process of executing a plurality of sequential pops of data from said stack to a plurality of registers starting from register 0 to a register specified by said final register number, based on the contents of a memory address specified by said dedicated stack pointer register.

4. The data processing circuit as defined in any one of claims 1 to 3, further comprising:

a program counter register (12) used only for the program counter;

wherein said group of dedicated stack pointer instructions comprises branch instructions that are an instruction for branching to a subroutine and a return instruction from said subroutine;
said decoding means (20) decodes said branch instructions;
said execution means (10) comprises:

means for executing at least one of a process of saving the contents of said program counter register (12) to a given second area of said stack provided in memory and a process of restoring the contents of said second area to said program counter register (12), based on a memory address specified by said dedicated stack pointer register, during the execution of said branch instruction; and
means for updating the contents of said dedicated stack pointer register (12) based on said saving and restoration.

5. The data processing circuit as defined in any one of claims 1 to 4, wherein said circuit uses instructions of a reduced instruction set computer.

6. The data processing circuit as defined in any one of claims 1 to 5, wherein:

a fixed-length instruction is decoded and execution is based on said fixed-length instruction.

7. A microcomputer comprising the data processing circuit as defined in any one of claims 1 to 6, storage means, and input and output means for inputting data from and for outputting data to external devices.

8. The microcomputer as defined in claim 7,
wherein a program that is executed thereby uses a program language that secures a storage region for auto-variables by using said stack pointer.

9. Electronic equipment comprising the microcomputer defined in claim 7 or 8.

Patentansprüche

1. Datenverarbeitungsschaltung, aufweisend:

ein zweckgebundenes Stapelzeigerregister, das nur für den Stapelzeiger (14) benutzt wird;
eine Dekodiereinrichtung (20) zum Dekodieren von Objektcode einer Gruppe zweckgebundener Stapelzeigerbefehle, die einen Objektcode haben, der das zweckgebundene Stapelzeigerregister als einen implizierten Operanden spezifiziert, und sich auf das Verarbeiten aufgrund des zweckgebundenen Stapelzeigerregisters beziehen, sowie zum Ausgeben eines Steuersignals aufgrund des Objektcodes,
eine Ausführungseinrichtung (10) zum Ausführen der Gruppe zweckgebundener Stapelzeigerbefehle aufgrund des Steuersignals und des Inhalts des zweckgebundenen Stapelzeigerregisters; und
eine Vielzahl von Registern (11), die in einer aneinandergrenzenden Folge vorgesehen sind, wobei die Gruppe zweckgebundener Stapelzeigerbefehle mindestens einen von zwei Befehlen, nämlich einen sequentiellen Push-Befehl und einen sequentiellen Pop-Befehl, aufweist, die Daten zum Spezifizieren einer Vielzahl von Registern in ihrem Objektcode haben;

wobei die Dekodiereinrichtung (20) mindestens einen der beiden Befehle, nämlich den sequentiellen Push-Befehl und den sequentiellen Pop-Befehl, dekodiert; und
die Ausführungseinrichtung (10), während der Ausführung mindestens eines der beiden Befehle, des sequentiellen Push-Befehls und des sequentiellen Pop-Befehls, mindestens einen von zwei Prozessen, nämlich einen Prozeß der Ausführung einer Vielzahl sequentieller Pushs von Daten aus der Vielzahl von Registern auf einen im Speicher vorgesehenen Stapel und einen Prozeß der Ausführung einer Vielzahl sequentieller Pops von Daten von dem Stapel an die Vielzahl von Registern, aufgrund des Inhalts einer von dem zweckgebundenen Stapelzeigerregister (14) spezifizierten Speicheradresse und der Daten zum Spezifizieren einer Vielzahl von Registern, durchführt;
dadurch gekennzeichnet, daß die Ausführungseinrichtung (10) folgendes aufweist:

eine Schreibeinrichtung zum Schreiben des Inhalts eines gegebenen Registers, welches eines der Vielzahl von Registern (11) ist, in einen im Speicher (50B) vorgesehenen Stapel aufgrund einer von dem zweckgebundenen Stapelzeigerregister (14) spezifizierten Speicheradresse;
eine Schreibfrequenz-Zähleinrichtung (46), die zählt, wie oft die Schreibeinrichtung geschrieben hat; und
eine Vergleichseinrichtung (45), die die von der Zähleinrichtung gezählte Schreibfrequenz mit dem Wert der Daten zum Spezifizieren einer Vielzahl von Registern vergleicht;

wobei die Schreibeinrichtung folgendes aufweist:

eine Schreibspeicheradressen-Generatoreinrichtung (30, 32), die eine erste Eingabe und eine zweite Eingabe durch einen Addierer summiert und eine Schreibspeicheradresse generiert, um ein Schreibziel zu spezifizieren;
eine erste Eingabesteuereinrichtung (45), die eine derartige Steuerung bietet, daß die erste Eingabe des Addierers der Inhalt des zweckgebundenen Stapelzeigerregisters beim Start der Ausführung eines sequentiellen zweckgebundenen Befehls ist und eine Schreibadresse ist, die anschließend von einer Schreibadressengeneratoreinrichtung generiert wird;
eine zweite Eingabesteuereinrichtung (45), die an den zweiten Eingang des Addierers einen Versatz ausgibt, der beim Schreiben eines Wortes an den Stapel benutzt wird; und
eine Schreibeinrichtung (45), die in den Stapel den Inhalt eines durch Subtraktionsverarbeitung spezifizierten Registers schreibt, für die die Daten zum Spezifizieren einer Vielzahl von Registern und die Schreibfrequenz aufgrund der Schreibspeicheradresse benutzt wird;

wodurch das Schreiben des Inhalts der Vielzahl von Registern in den Stapel und das Beenden des Schreibens aufgrund des Vergleichsergebnisses der Vergleichseinrichtung gesteuert werden.

2. Datenverarbeitungsschaltung, aufweisend:

ein zweckgebundenes Stapelzeigerregister, das nur für den Stapelzeiger (14) benutzt wird;
eine Dekodiereinrichtung (20) zum Dekodieren von Objektcode einer Gruppe zweckgebundener Stapelzeigerbefehle, die einen Objektcode haben, der das zweckgebundene Stapelzeigerregister als einen implizierten Operanden spezifiziert, und sich auf das Verarbeiten aufgrund des zweckgebundenen Stapelzeigerregisters beziehen, sowie zum Ausgeben eines Steuersignals aufgrund des Objektcodes,
eine Ausführungseinrichtung (10) zum Ausführen der Gruppe zweckgebundener Stapelzeigerbefehte aufgrund des Steuersignals und des Inhalts des zweckgebundenen Stapelzeigerregisters; und
eine Vielzahl von Registern (11), die in einer aneinandergrenzenden Folge vorgesehen sind,

wobei die Gruppe zweckgebundener Stapelzeigerbefehle mindestens einen von zwei Befehlen, nämlich einen sequentiellen Push-Befehl und einen sequentiellen Pop-Befehl, aufweist, die Daten zum spezifizieren einer Vielzahl von Registern in ihrem Objektcode haben;
wobei die Dekodiereinrichtung (20) mindestens einen der beiden Befehle, nämlich den sequentiellen Push-Befehl und den sequentiellen Pop-Befehl, dekodiert; und
die Ausführungseinrichtung (10), während der Ausführung mindestens eines der beiden Befehle, des sequentiellen Push-Befehls und des sequentiellen Pop-Befehls, mindestens einen von zwei Prozessen, nämlich einen Prozeß der Ausführung einer Vielzahl sequentieller Pushs von Daten aus der Vielzahl von Registern auf einen im Speicher vorgesehenen Stapel und einen Prozeß der Ausführung einer Vielzahl sequentieller Pops von Daten von dem Stapel an die Vielzahl von Registern, aufgrund des Inhalts einer von dem zweckgebundenen Stapelzeigerregister (14) spezifizierten Speicheradresse und der Daten zum Spezifizieren einer Vielzahl von Registern durchführt;
dadurch gekennzeichnet, daß die Ausführungseinrichtung (10) folgendes aufweist:

eine Leseeinrichtung zum Lesen des Inhalts eines im Speicher vorgesehenen Stapels aufgrund einer von dem zweckgebundenen Stapelzeigerregister spezifizierten Speicheradresse und zum Speichern des Inhalts in einem gegebenen Register der Vielzahl von Registern;
eine Lesefrequenz-Zähleinrichtung, die zählt, wie oft die Leseeinrichtung gelesen hat; und
eine Vergleichseinrichtung (45), die die von der Zähleinrichtung gezählte Lesefrequenz mit dem Wert der Daten zum Spezifizieren einer Vielzahl von Registern vergleicht;

wobei die Leseeinrichtung folgendes aufweist:

eine erste Eingabesteuereinrichtung (45), die eine derartige Steuerung bietet, daß die erste Eingabe eines Addierers der Inhalt des zweckgebundenen Stapelzeigerregisters beim Start der Ausführung eines sequentiellen zweckgebundenen Befehls ist und eine Lesespeicheradresse ist, die anschließend von einer Leseadressengeneratoreinrichtung generiert wird;
eine zweite Eingabesteuereinrichtung (45), die an den zweiten Eingabe des Addierers einen Versatz ausgibt, der beim Lesen eines Wortes von dem Stapel benutzt wird; und
eine Leseeinrichtung (45), die den Inhalt des Stapels aufgrund der Lesespeicheradresse liest und den Inhalt in einem Register speichert, das aufgrund der Lesefrequenz spezifiziert wurde,

wodurch das Lesen des Inhalts des Stapels und das Beenden des Lesens aufgrund des Vergleichsergebnisses der Vergleichseinrichtung gesteuert werden.

3. Datenverarbeitungsschaltung nach Anspruch 1 oder 2, ferner aufweisend:

n Mehrzweck-Register (11), die durch Registernummern 0 bis n-1 spezifiziert sind;

wobei der Objektcode mindestens eines der beiden Befehle, des sequentiellen Push-Befehls und des sequentiellen Pop-Befehls, als Daten zum Spezifizieren einer Vielzahl von Registern eine letzte Registernummer umfaßt, auf die eine der Registernummern spezifiziert ist; und
die Ausführungseinrichtung (10) mindestens einen von zwei Prozessen, nämlich einen Prozeß der Ausführung einer Vielzahl sequentieller Pushs von Daten auf einen im Speicher vorgesehenen Stapel von einer Vielzahl

von Registern, beginnend mit dem Register 0 bis zu einem von der letzten Registernummer spezifizierten Register, und einen Prozeß zur Ausführung einer Vielzahl sequentieller Pops von Daten aus dem Stapel zu einer Vielzahl von Registern, beginnend mit dem Register 0 bis zu einem von der letzten Registernummer spezifizierten Register, aufgrund des Inhalts einer Speicheradresse durchführt, die von dem zweckgebundenen Stapelzeigerregister spezifiziert ist.

4. Datenverarbeitungsschaltung nach einem der Ansprüche 1 bis 3, ferner aufweisend:

ein Programmzählerregister (12), welches nur für den Programmzähler verwendet wird;

wobei die Gruppe zweckgebundener Stapelzeigerbefehle Verzweigungsbefehle aufweist, die ein Befehl zum Abzweigen zu einer Subroutine und ein Rückkehrbefehl von der Subroutine sind;
die Dekodiereinrichtung (20) die Verzweigungsbefehle dekodiert; und
die Ausführungseinrichtung (10) folgendes aufweist:

eine Einrichtung zur Ausführung mindestens eines von zwei Prozessen, nämlich eines Prozesses der Sicherung des Inhalts des Programmzählerregisters (12) zu einem gegebenen zweiten Bereich des im Speicher vorgesehenen Stapels und eines Prozesses zum Wiederherstellung des Inhalts des zweiten Bereiches in dem Programmzählerregister (12) aufgrund einer von dem zweckgebundenen Stapelzeigerregister spezifizierten Speicheradresse während der Ausführung des Verzweigungsbefehls; und
eine Einrichtung zum Aktualisieren des Inhalts des zweckgebundenen Stapelzeigerregisters (12) aufgrund der Sicherung und Wiederherstellung.

5. Datenverarbeitungsschaltung nach einem der Ansprüche 1 bis 4, bei der die Schaltung Befehle eines reduzierten Befehlssatzrechners benutzt.

6. Datenverarbeitungsschaltung nach einem der Ansprüche 1 bis 5, bei der ein Befehl fester Länge dekodiert wird und die Ausführung auf dem Befehl fester Länge beruht.

7. Mikrorechner mit der Datenverarbeitungsschattung nach einem der Ansprüche 1 bis 6, einer Speichereinrichtung und Eingabe- und Ausgabeeinrichtungen zur Eingabe von Daten von und zur Ausgabe von Daten an externe Vorrichtungen.

8. Mikrorechner nach Anspruch 7, bei dem ein Programm, das von ihm ausgeführt wird, eine Programmsprache benutzt, die eine Speicherzone für Auto-Variable durch Benutzung des Stapelzeigers sicherstellt.

9. Elektronisches Gerät, welches den in Anspruch 7 oder 8 beschriebenen Mikrorechner aufweist.

Revendications

1. Circuit de traitement de données comprenant :

un registre dédié de pointeur de pile, qui est utilisé uniquement pour le pointeur (14) de pile ;
un moyen (20) de décodage, destiné à décoder un code objet d'un groupe d'instructions dédié de pointeur de pile qui comportent un code objet spécifiant le registre dédié de pointeur de pile, en tant qu'opérande implicite et qui se rapportent à un traitement fondé sur le registre dédié de pointeur de pile, et destiné à délivrer un signal de commande, sur la base du code objet,
un moyen (10) d'exécution destiné à exécuter le groupe d'instructions dédié de pointeur de pile, sur la base du signal de commande et du contenu du registre dédié de pointeur de pile; et
une pluralité (11) de registres, prévue dans une suite contiguë, dans laquelle le groupe d'instructions dédié de pointeur de pile comprend au moins l'une d'une instruction de chargement séquentiel et d'une instruction de déchargement séquentiel comportant des données destinées à spécifier une pluralité de registres dans le code objet de celle-ci ;
le moyen (20) de décodage décode au moins l'une de l'instruction de chargement séquentiel et de l'instruction de déchargement séquentiel ; et
le moyen (10) d'exécution effectue au moins l'un d'un traitement consistant à exécuter une pluralité de chargements séquentiels de données, à partir de la pluralité de registres, dans une pile prévue dans la mémoire,

et d'un traitement consistant à exécuter une pluralité de déchargements séquentiels de données, à partir de la pile, dans la pluralité de registres, sur la base du contenu d'une adresse en mémoire spécifiée par le registre (14) dédié de pointeur de pile et des données destinées à spécifier une pluralité de registres, pendant l'exécution d'au moins l'une de l'instruction de chargement séquentiel et de l'instruction de déchargement séquentiel ;

caractérisé en ce que :

le moyen (10) d'exécution comprend :

un moyen d'écriture destiné à écrire le contenu d'un registre donné qui est l'un des registres parmi la pluralité (11) de registres, dans une pile prévue dans la mémoire (50B), sur la base d'une adresse en mémoire spécifiée par le registre (14) dédié du pointeur de pile;
un moyen (46) de comptage du nombre de fois d'écriture, destiné à compter le nombre d'écriture du moyen d'écriture ; et
un moyen (45) de comparaison destiné à comparer le nombre de fois d'écriture comptée par le moyen de comptage, à la valeur des données destinées à spécifier une pluralité de registres ;

dans lequel le moyen d'écriture comprend :

des moyens (30, 32) de production d'adresses d'écriture en mémoire, destinés à additionner une première entrée et une deuxième entrée, au moyen d'un additionneur et à produire une adresse d'écriture en mémoire, destinée à spécifier une destination d'écriture ;
un moyen (45) de commande de première entrée, destiné à délivrer une commande telle que la première entrée de l'additionneur est le contenu du registre dédié du pointeur de pile, au démarrage de l'exécution d'une instruction séquentielle spécialisée, et est une adresse d'écriture produite ultérieurement par un moyen de production d'adresses d'écriture ;
un moyen (45) de commande de deuxième entrée, destiné à délivrer un décalage utilisé pendant l'écriture d'un mot dans la pile, à la deuxième entrée de l'additionneur ; et
un moyen (45) d'écriture destiné à écrire dans la pile le contenu d'un registre spécifié, par un traitement de soustraction qui utilise les données destinées à spécifier une pluralité de registres et le nombre de fois d'écriture, sur la base de l'adresse d'écriture en mémoire ;
de sorte que l'écriture du contenu de la pluralité de registres, dans la pile et l'achèvement de l'écriture sont commandés sur la base du résultat de comparaison du moyen de comparaison.

2. Circuit de traitement de données comprenant :

un registre dédié de pointeur de pile qui est utilisé uniquement pour le pointeur (14) de pile ;
un moyen (20) de décodage destiné à décoder un code objet d'un groupe d'instructions dédiées de pointeur de pile qui comportent un code objet spécifiant le registre dédié de pointeur de pile, en tant qu'opérande implicite et qui se rapportent à un traitement fondé sur le registre dédié de pointeur de pile, et destiné à délivrer un signal de commande, sur la base du code objet ;
moyen (10) d'exécution destiné à exécuter le groupe d'instructions dédiées de pointeur de pile, sur la base du signal de commande et du contenu du registre dédié de pointeur de pile; et
une pluralité (11) de registres, prévue dans une suite contiguë,

dans lequel le groupe d'instructions dédiées de pointeur de pile comprend au moins l'une d'une instruction de chargement séquentiel et une instruction de déchargement séquentiel comportant des données destinées à spécifier une pluralité de registres dans le code objet de celle-ci;

le moyen (20) de décodage décode au moins l'une de l'instruction de chargement séquentiel et de l'instruction de déchargement séquentiel ; et

le moyen (10) d'exécution effectue au moins l'un d'un traitement consistant à exécuter une pluralité de chargements séquentiels de données, à partir de la pluralité de registres, dans une pile prévue dans la mémoire et d'un traitement destiné à exécuter une pluralité de déchargements séquentiels de données, à partir de la pile, dans la pluralité de registres, sur la base du contenu d'une adresse en mémoire spécifiée par le registre (14) dédié du pointeur de pile et des données destinées à spécifier une pluralité de registres, pendant l'exécution d'au moins l'une de l'instruction de chargement séquentiel et de l'instruction de déchargement séquentiel;

caractérisé en ce que :

le moyen (10) d'exécution comprend :

un moyen de lecture destiné à lire le contenu d'une pile, prévue dans la mémoire, sur la base d'une adresse en mémoire spécifiée par le registre dédié du pointeur de pile, et destiné à mémoriser le contenu dans un registre donné de la pluralité de registres ;
un moyen de comptage de nombre de lecture destiné à compter le nombre de fois de lecture du moyen de lecture ; et
un moyen (45) de comparaison destiné à comparer le nombre de lecture compté par le moyen de comptage, à la valeur des données destinées à spécifier une pluralité de registres ;

dans lequel le moyen de lecture comprend:

un moyen (45) de commande de première entrée, destiné à délivrer une commande telle que la première entrée d'un additionneur est le contenu du registre dédié du pointeur de pile, au démarrage de l'exécution d'une instruction séquentielle spécialisée, et est une adresse de lecture en mémoire, calculée ultérieurement par un moyen de production d'adresse de lecture ;
un moyen (45) de commande de deuxième entrée, destiné à délivrer un décalage utilisé pendant la lecture d'un mot à partir de la pile, à la deuxième entrée de l'additionneur ;
un moyen (45) de lecture destiné à lire le contenu de la pile, sur la base de l'adresse de lecture en mémoire et à mémoriser le contenu dans un registre spécifié sur la base du nombre de fois de lecture;
de sorte que la lecture du contenu de la pile et l'achèvement de la lecture sont commandés sur la base du résultat de comparaison du moyen de comparaison.

3. Circuit de traitement de données, suivant la revendication 1 ou 2 comprenant, en outre :

n registres (11) non spécialisés, spécifiée par les numéros de registres 0 à n-1 ;

dans lequel le code objet d'au moins l'une de l'instruction de chargement séquentiel et de l'instruction de déchargement séquentiel, comprend un numéro de registre final auquel l'un des numéros de registre est spécifié, en tant que données destinées à spécifier une pluralité de registres ; et
le moyen (10) d'exécution effectue au moins l'un d'un traitement consistant à exécuter une pluralité de chargements séquentiels de données dans une pile prévue dans la mémoire, à partir d'une pluralité de registres, du registre 0 à un registre spécifié par le numéro de registre final et d'un traitement consistant à exécuter une pluralité de déchargements séquentiels de données, de la pile dans une pluralité de registres, du registre 0 à un registre spécifié par le numéro de registre final, sur la base du contenu d'une adresse en mémoire spécifiée par le registre dédié de pointeur de pile.

4. Circuit de traitement de données, tel que défini dans l'une quelconque des revendications 1 à 3 comprenant, en outre :

un registre (12) compteur ordinal utilisé seulement pour le compteur ordinal ;

dans lequel le groupe d'instructions dédiées de pointeur de pile comprend des instructions de branchement qui sont une instruction de branchement à un sous-programme et une instruction de retour du sous-programme ;
le moyen (20) de décodage décode des instructions de branchement ;
le moyen (10) d'exécution comprend :

un moyen destiné à exécuter au moins un traitement consistant à sauvegarder le contenu du registre (12) compteur ordinal dans une deuxième zone donnée de la pile, prévue dans la mémoire ou un traitement consistant à restaurer le contenu de la deuxième zone dans le registre (12) compteur ordinal, sur la base d'une adresse en mémoire spécifiée par le registre (12) dédié du pointeur de pile, pendant l'exécution de l'instruction de branchement ; et
un moyen destiné à mettre à jour le contenu du registre (12) dédié de pointeur de pile, sur la base de la sauvegarde et de la restauration.

5. Circuit de traitement de données, tel que défini suivant l'une quelconque des revendications 1 à 4, dans lequel le circuit utilise des instructions d'un ordinateur à jeu d'instructions réduit.

6. Circuit de traitement de données, tel que défini suivant l'une quelconque des revendications 1 à 5, dans lequel :

une instruction de longueur fixe est décodée et l'exécution est fondée sur l'instruction de longueur fixe.

7. Micro-ordinateur comprenant le circuit de traitement de données, tel que défini suivant l'une quelconque des revendications 1 à 6, un moyen de mémorisation et des moyens d'entrée et de sortie, destinés à introduire des données à partir de dispositifs externes et à leur délivrer des données.

8. Micro-ordinateur tel que défini suivant la revendication 7,
dans lequel un programme qui est exécuté utilise ainsi un langage de programme qui réserve une zone de mémoire destinée à des variables automatiques, en utilisant le pointeur de pile.

9. Matériel électronique comprenant le micro-ordinateur défini à la revendication 7 ou 8.

FIG. 1

FIG.1A	FIG.1B

FIG. 1A

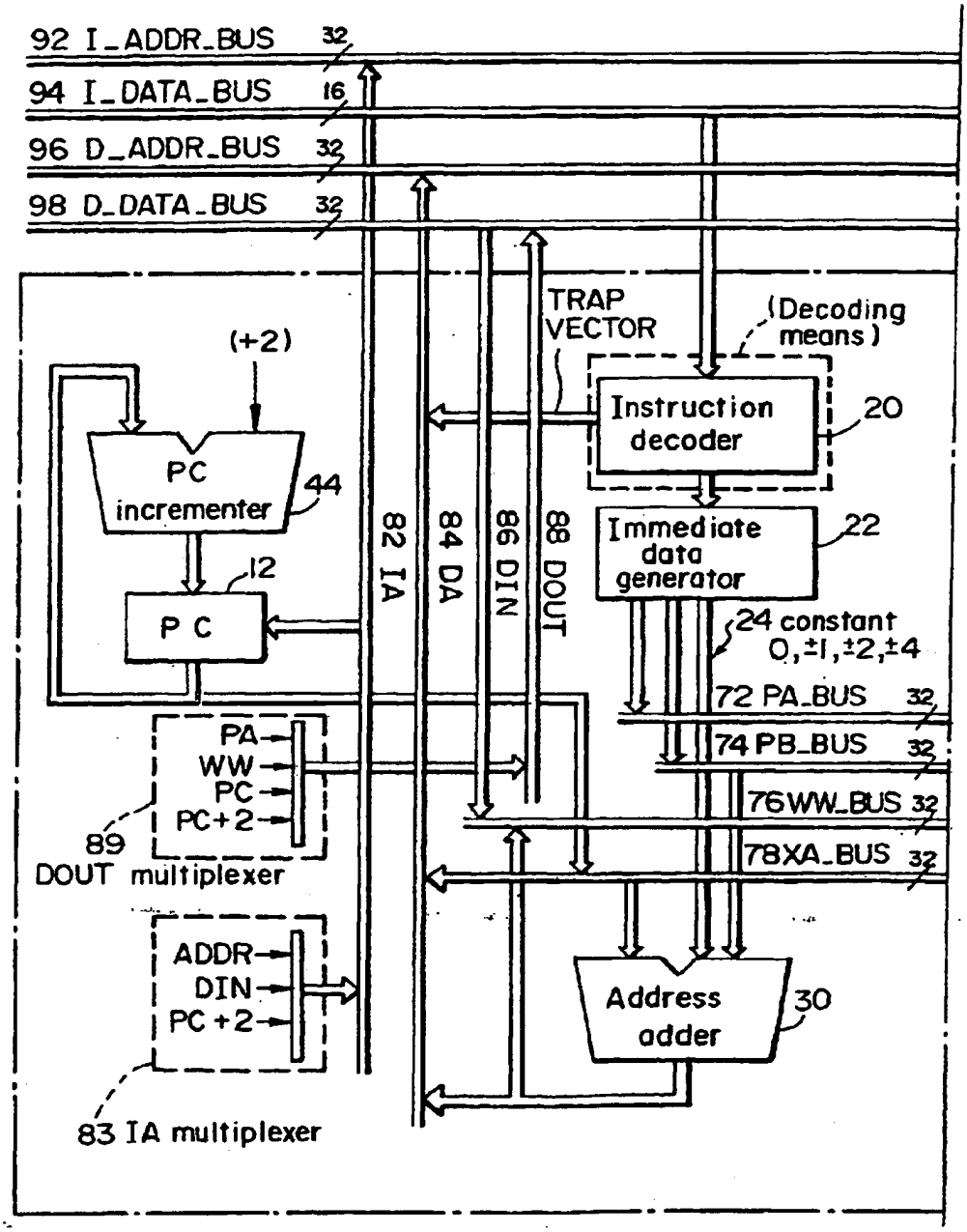


FIG. 1B

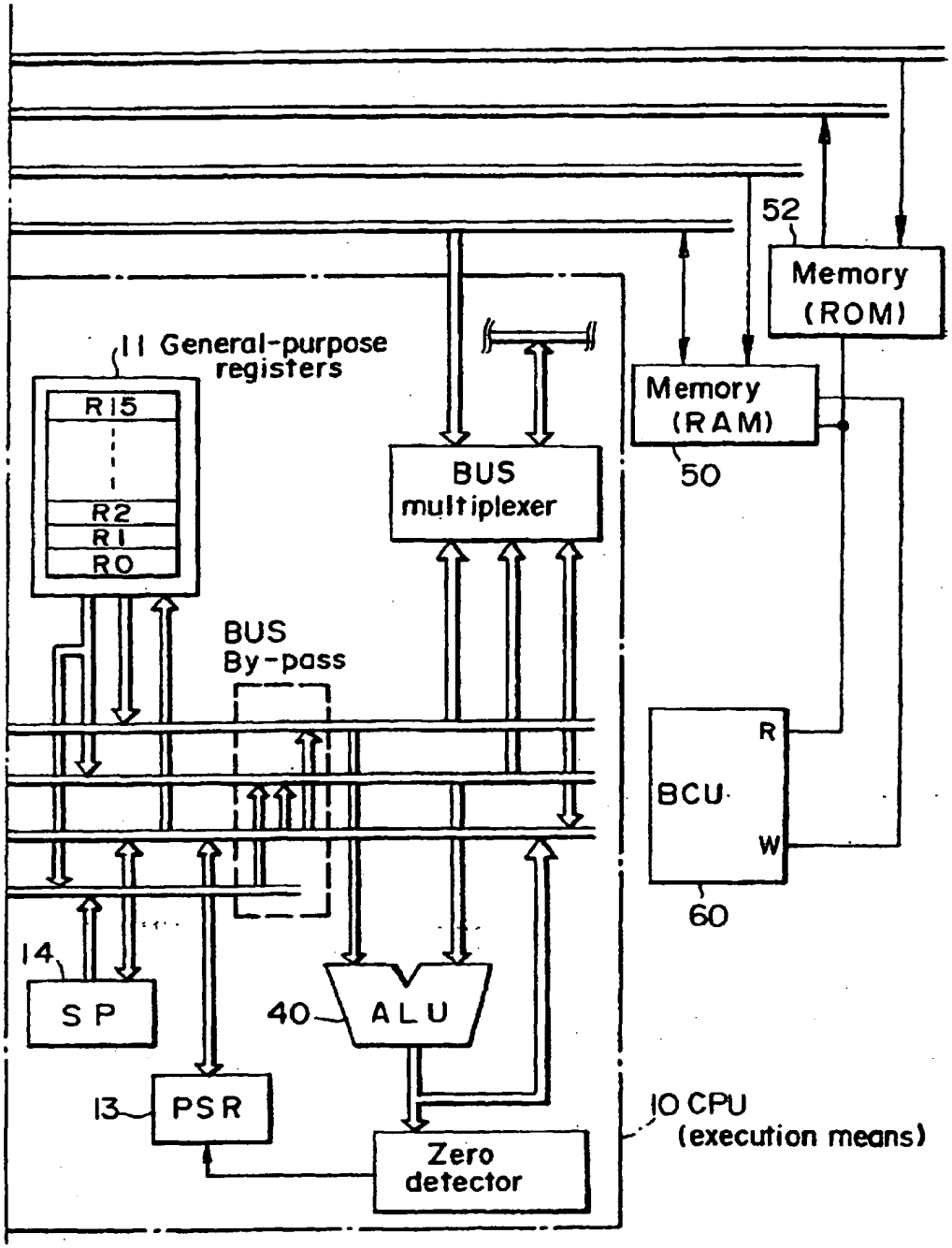

52
Memory
(ROM)
11 General-purpose
registers
R15
R2
R1
R0
Memory
(RAM)
50
BUS
multiplexer
BUS
By-pass
R
BCU
W
60
14
SP
40
ALU
13
PSR
Zero
detector
10 CPU
(execution means)

FIG.2

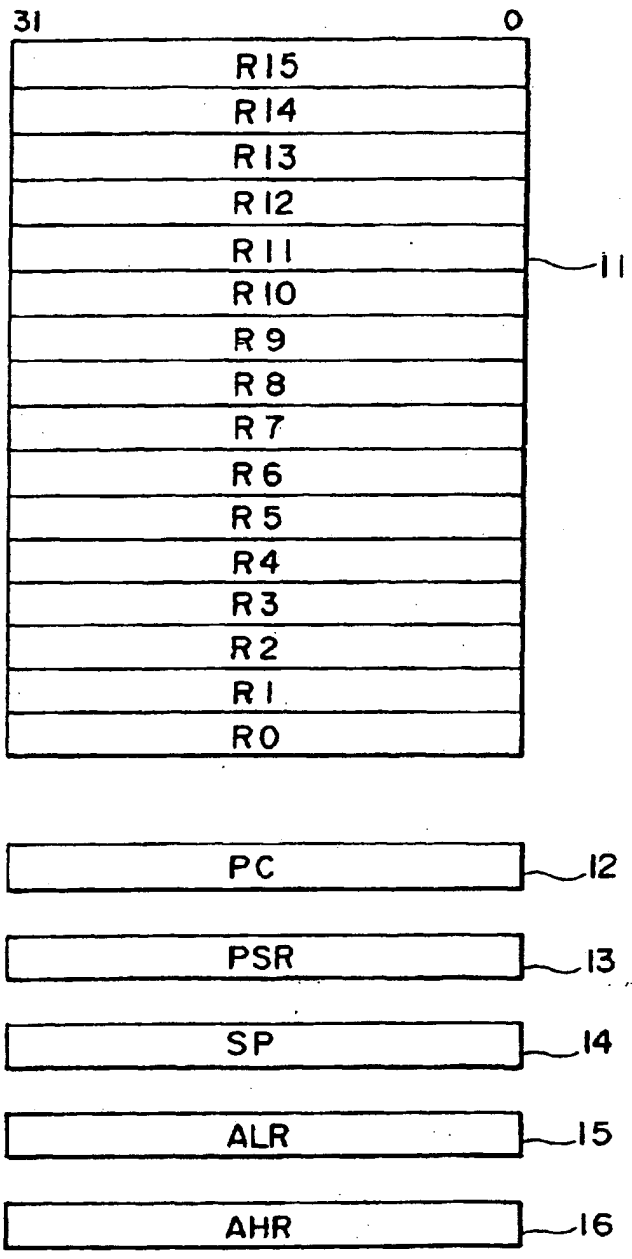

Register set
31
0
R15
R14
R13
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
R0
11
PC
12
PSR
13
SP
14
ALR
15
AHR
16

FIG. 3

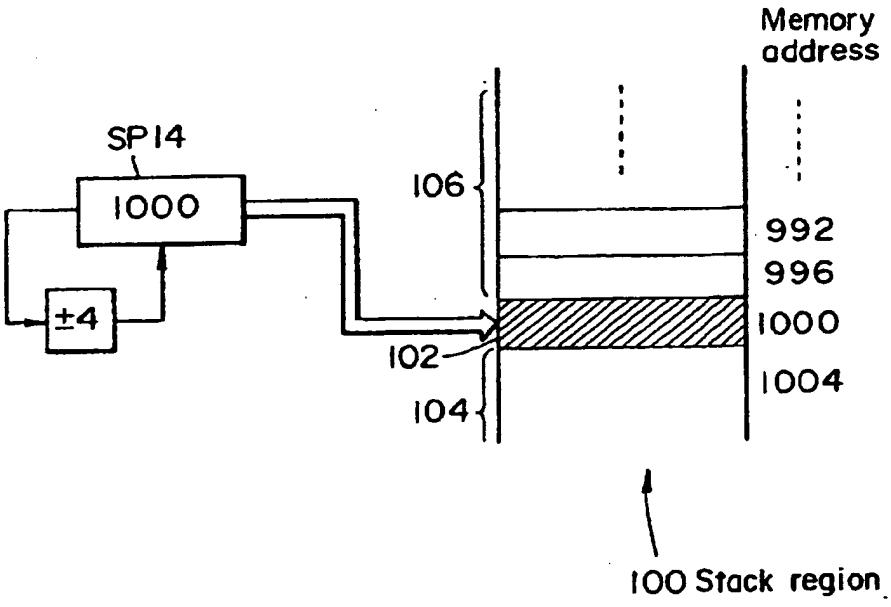
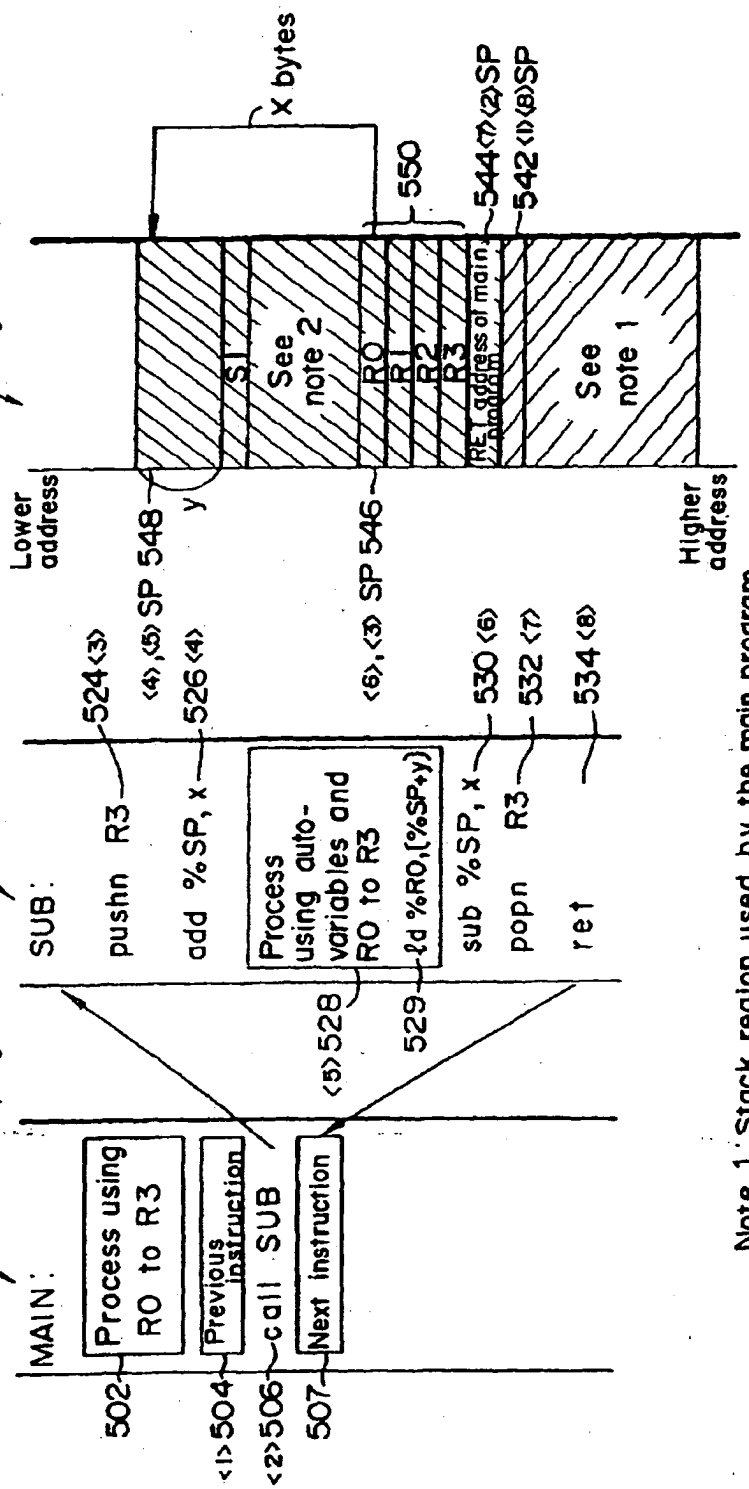

Memory address
SP 14
1000
±4
106
992
996
1000
1004
102
104
100 Stack region

FIG. 4



Note 1: Stack region used by the main program

Note 2: Auto-variable region used by the subroutine

FIG. 5

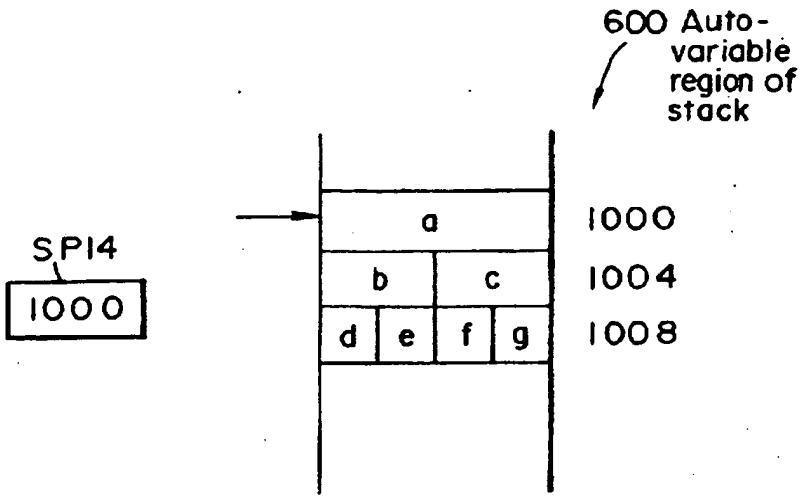

600 Auto-variable region of stack
SP14
1000
a
b
c
d
e
f
g
1000
1004
1008

FIG. 6A

SP-relative load instruction

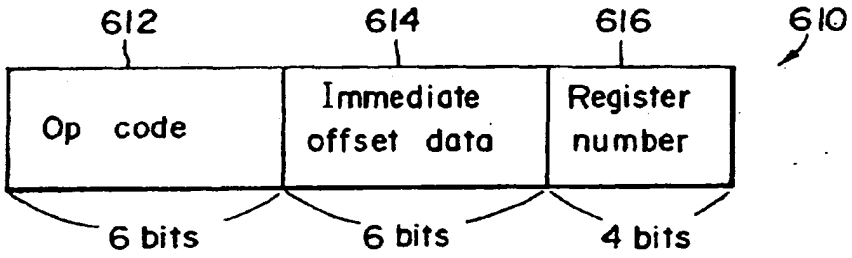


FIG. 6B

General-purpose load instruction

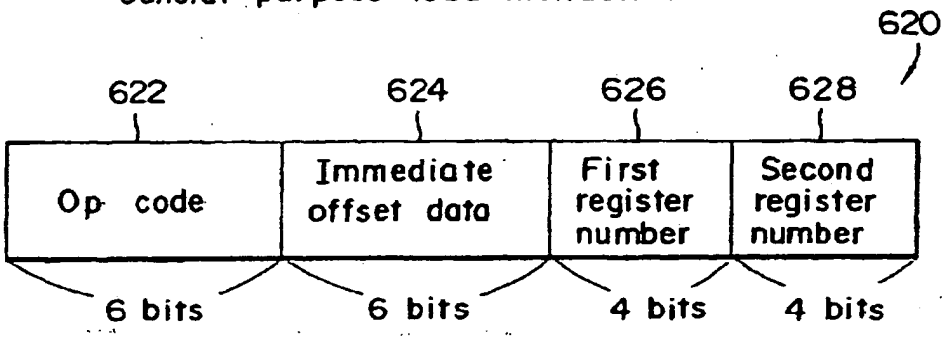


FIG. 7

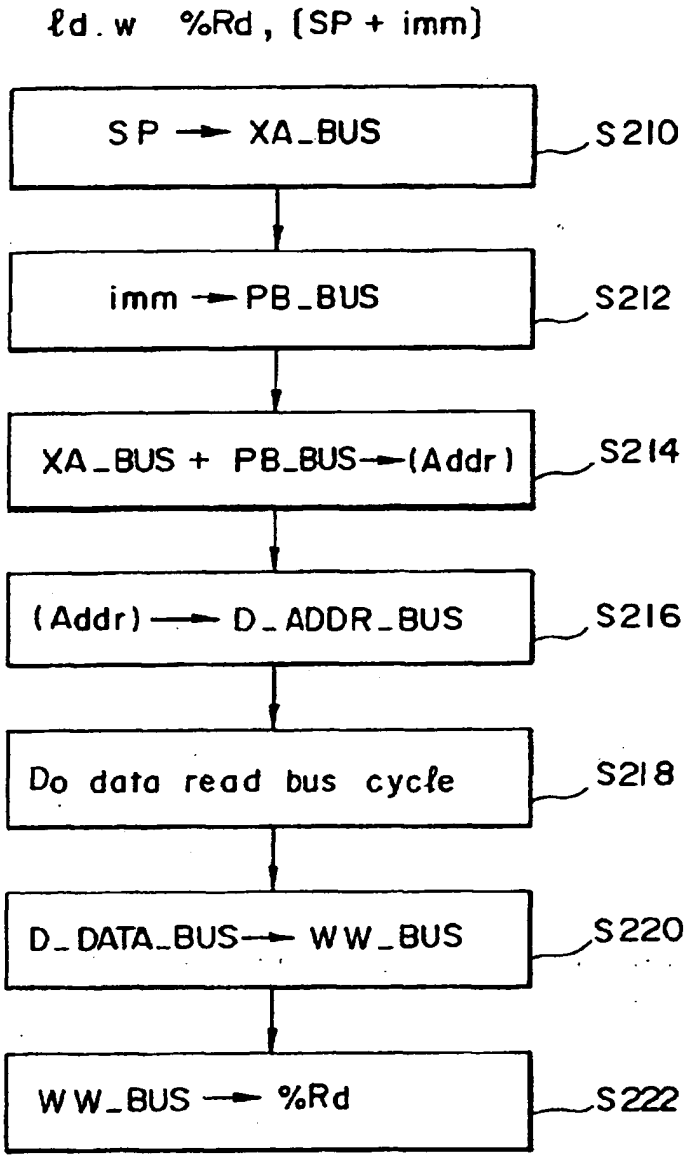
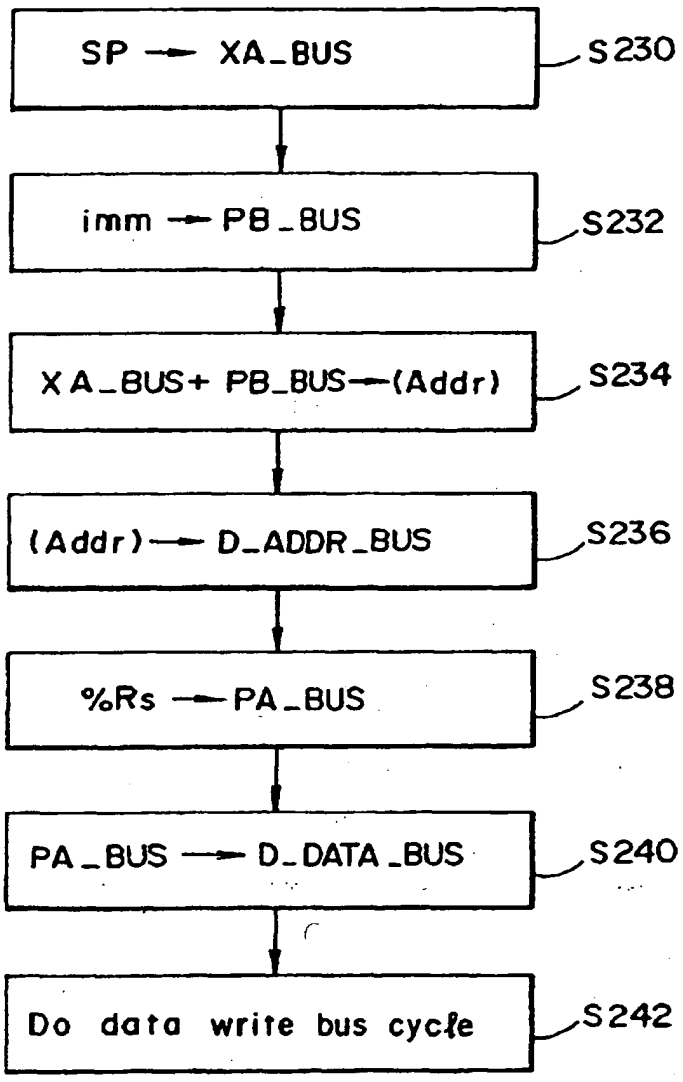

ℓd.w %Rd, [SP + imm]
SP → XA_BUS
S210
imm → PB_BUS
S212
XA_BUS + PB_BUS → (Addr)
S214
(Addr) → D_ADDR_BUS
S216
Do data read bus cycle
S218
D_DATA_BUS → WW_BUS
S220
WW_BUS → %Rd
S222

FIG. 8

ld.w [SP + imm], %Rs



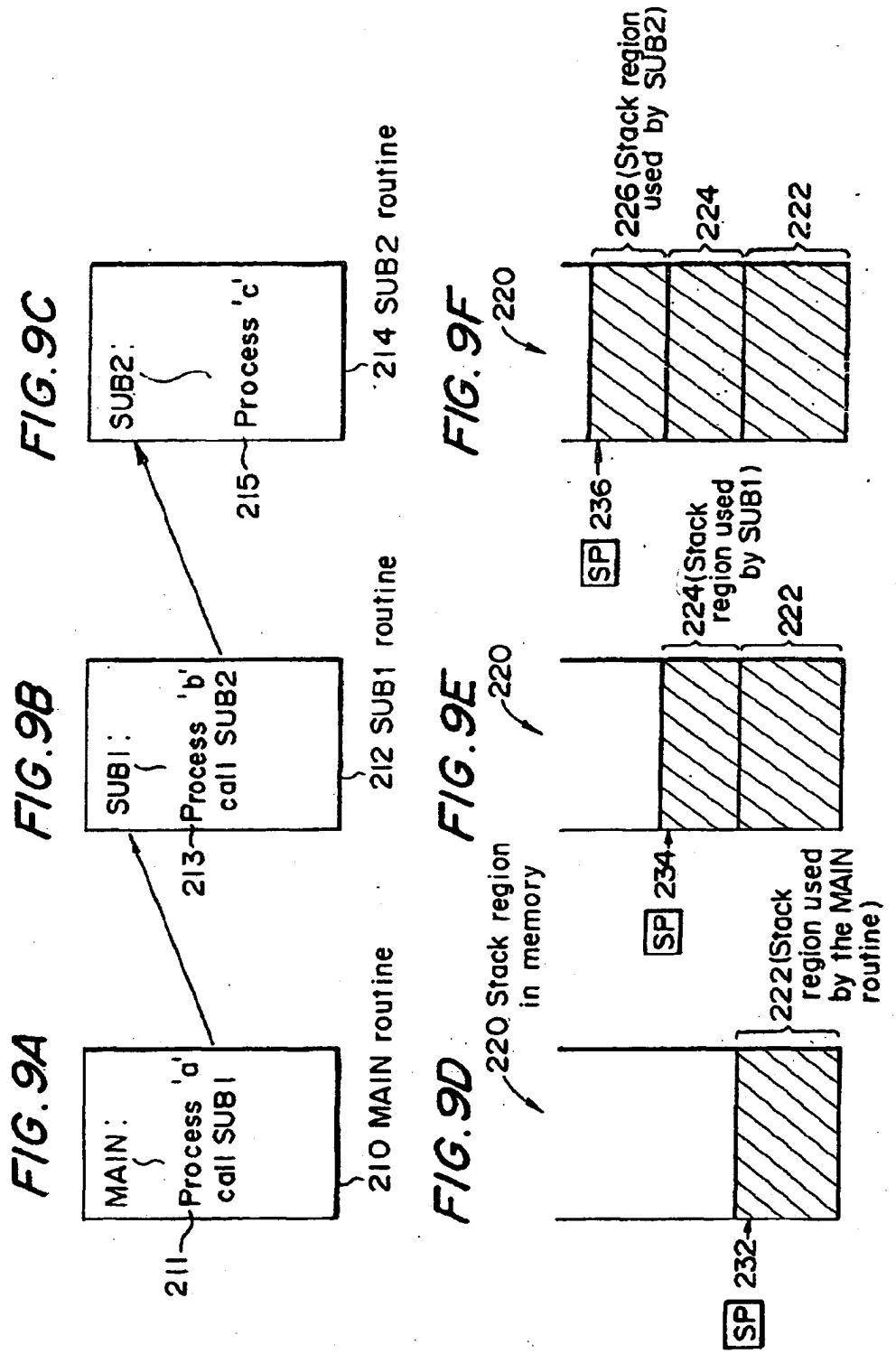


FIG. 9A
MAIN:
Process 'a'
call SUB1
211
210 MAIN routine
FIG. 9B
SUB1:
Process 'b'
call SUB2
213
212 SUB1 routine
FIG. 9C
SUB2:
Process 'c'
215
214 SUB2 routine
FIG. 9D
220 Stack region
in memory
SP 232
222 (Stack
region used
by the MAIN
routine)
FIG. 9E
220
SP 234
224 (Stack
region used
by SUB1)
222
FIG. 9F
220
SP 236
226 (Stack region
used by SUB2)
224
222

FIG. 10A

Stack pointer move instruction

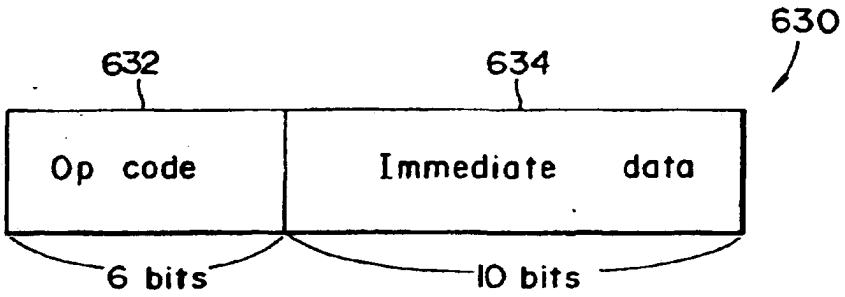


FIG. 10B

General immediate data arithmetic instruction

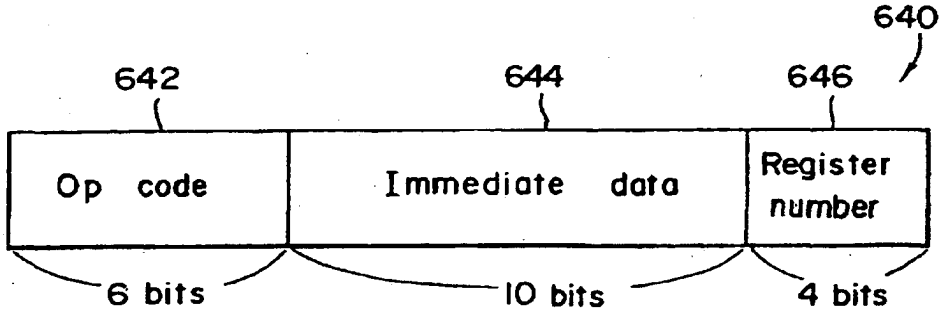


FIG. 11

Add to SP

add %SP , imm

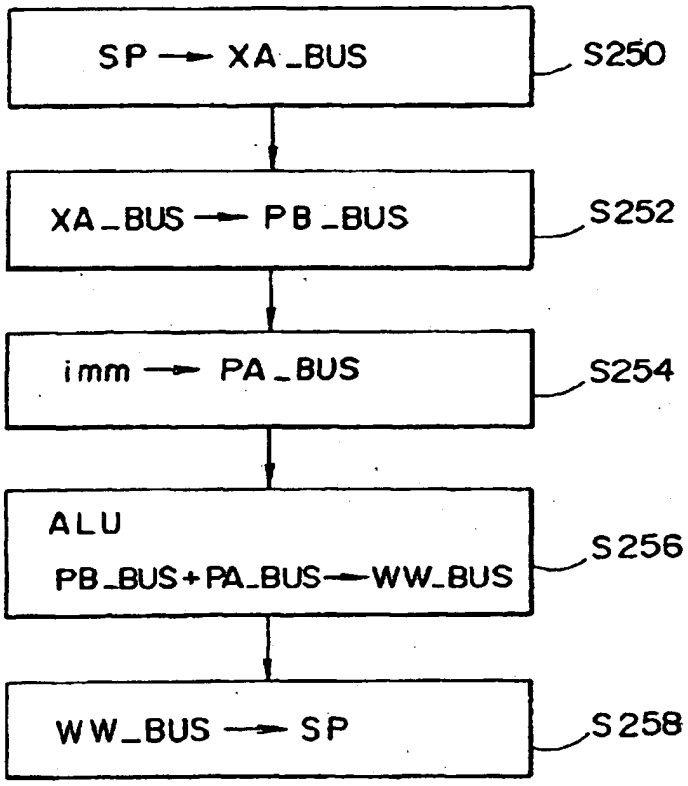


FIG. 12

sub %sp imm

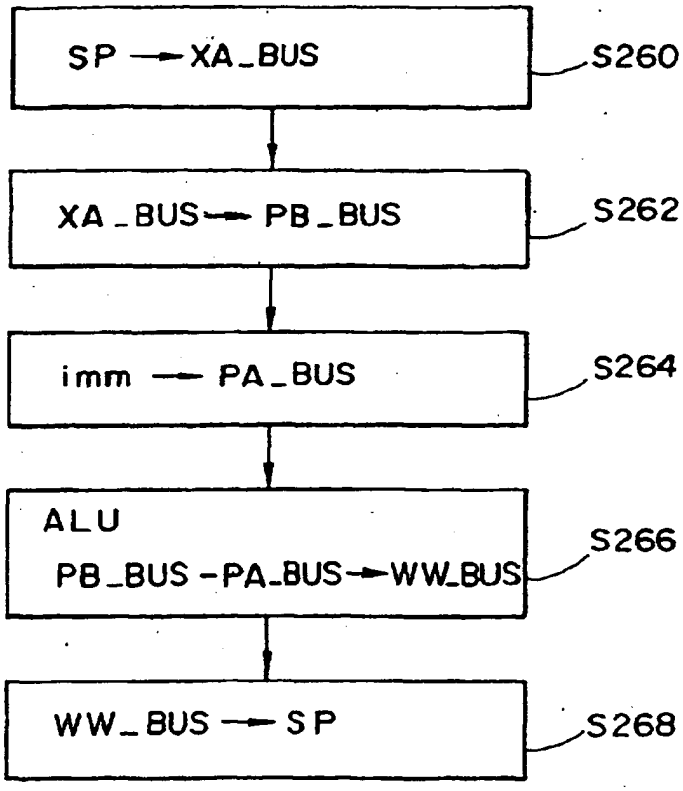


FIG. 13

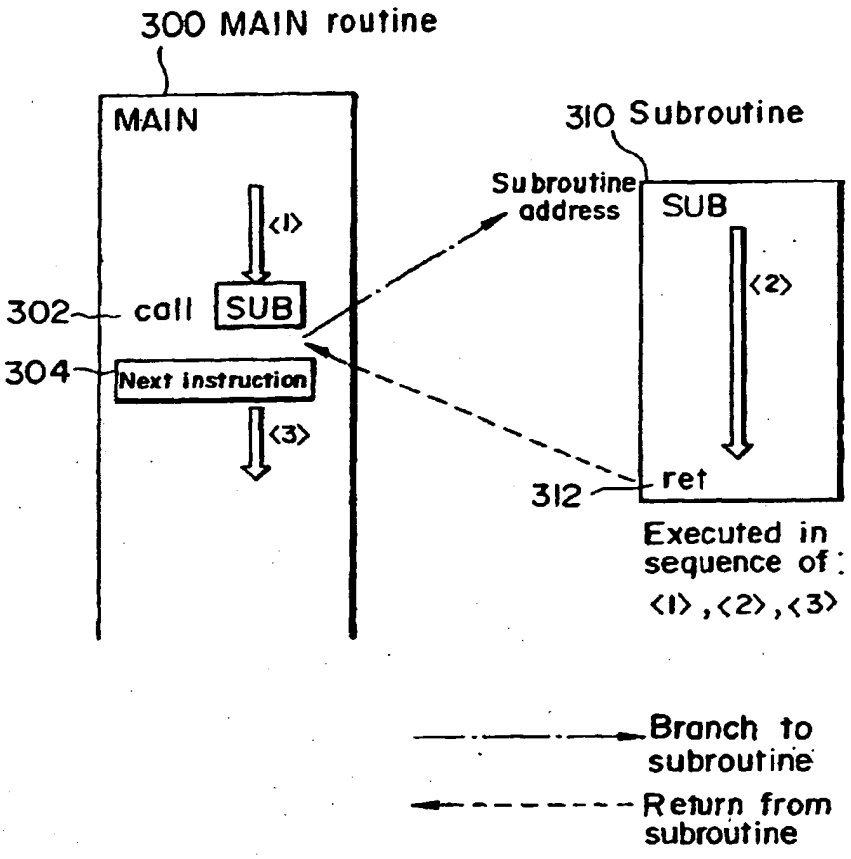

300 MAIN routine
MAIN
310 Subroutine
Subroutine address
SUB
<1>
<2>
302
call
SUB
304
Next instruction
<3>
312
ret
Executed in sequence of: <1>,<2>,<3>
Branch to subroutine
Return from subroutine

FIG. 14

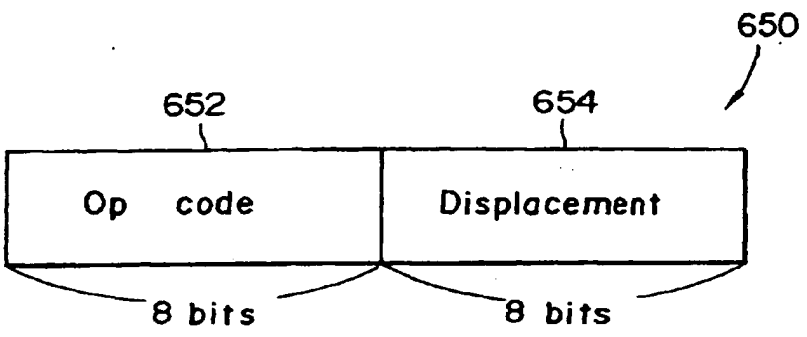

Branch instruction
650
652
654
Op code
Displacement
8 bits
8 bits

FIG. 15

call imm

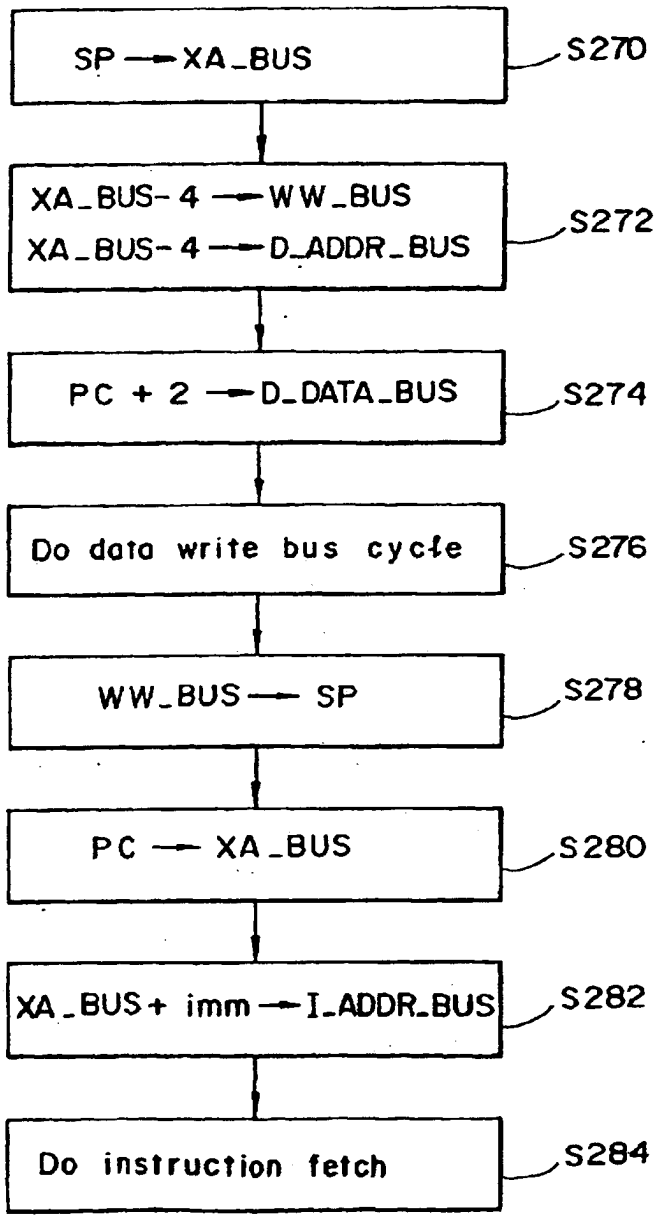


FIG. 16

ret

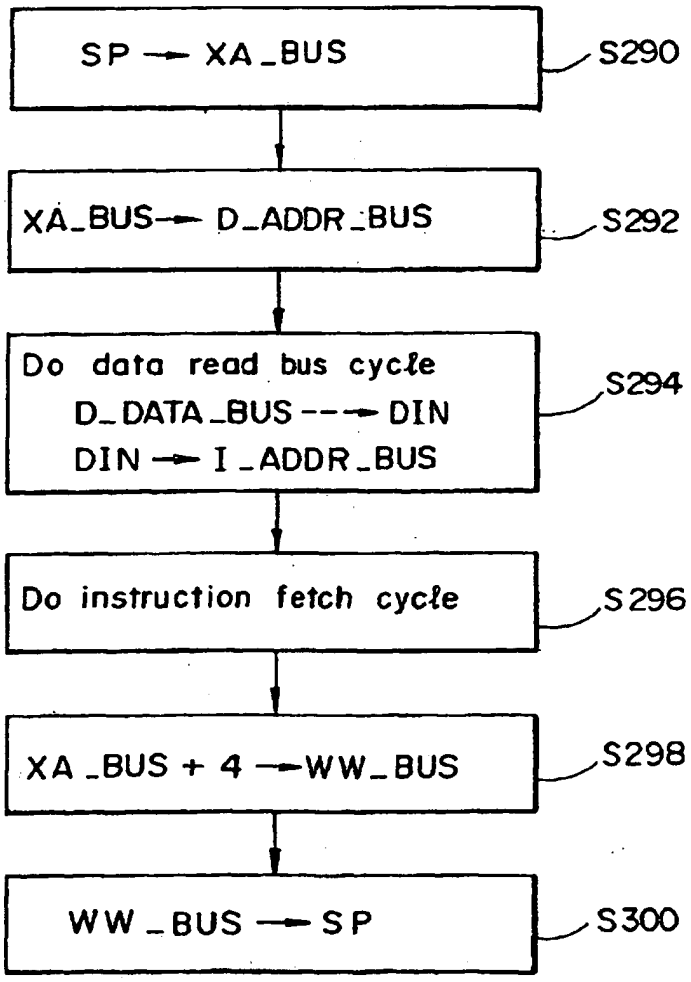

SP → XA_BUS
S290
XA_BUS → D_ADDR_BUS
S292
Do data read bus cycle
D_DATA_BUS ---→ DIN
DIN → I_ADDR_BUS
S294
Do instruction fetch cycle
S296
XA_BUS + 4 → WW_BUS
S298
WW_BUS → SP
S300

FIG. 17A

Execution of push R1

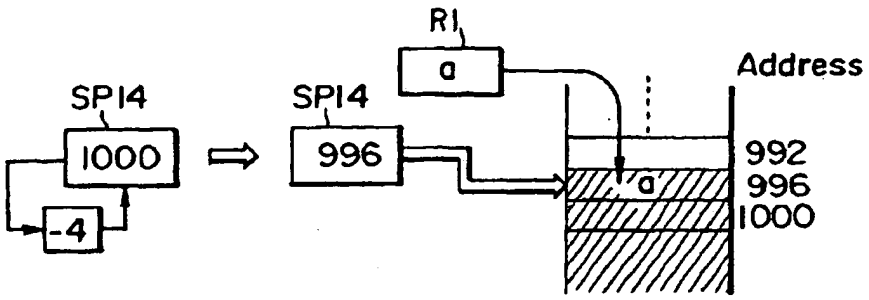


FIG. 17B

Execution of push R2

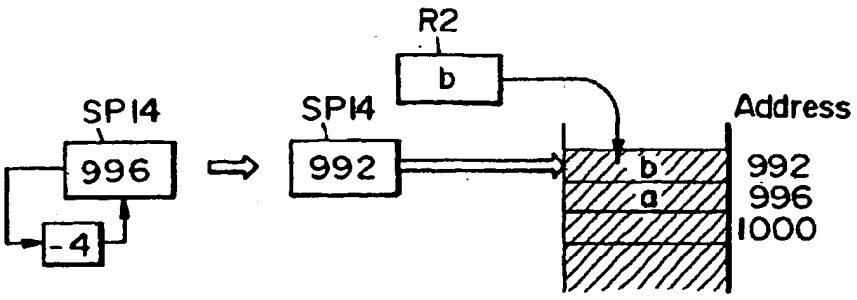


FIG. 18A

Execution of pop R2

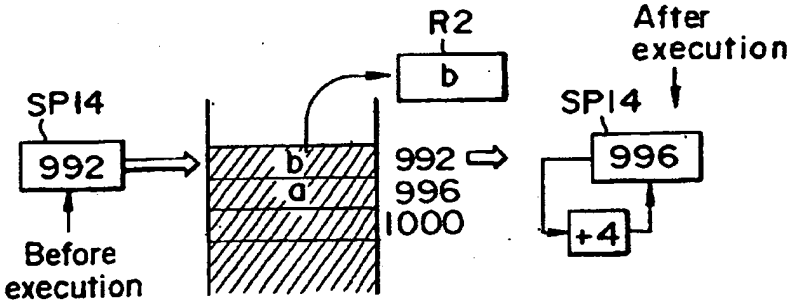


FIG. 18B

Execution of pop R1

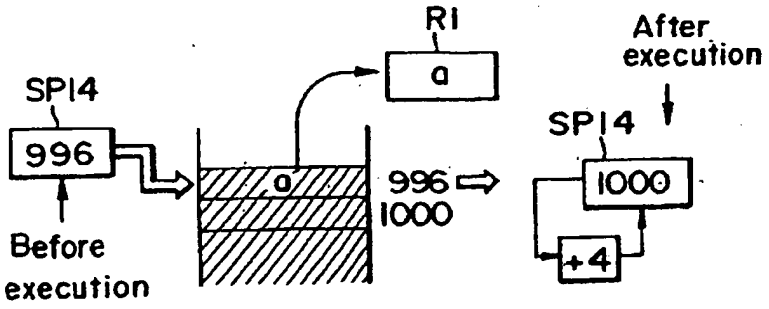
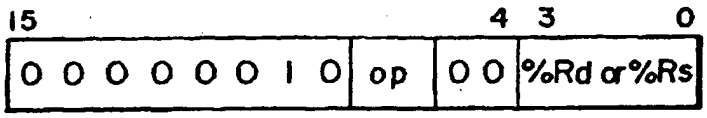


FIG. 19

pushn and popn instructions



Instruction	op
pushn	0 0
popn	0 1

FIG. 20

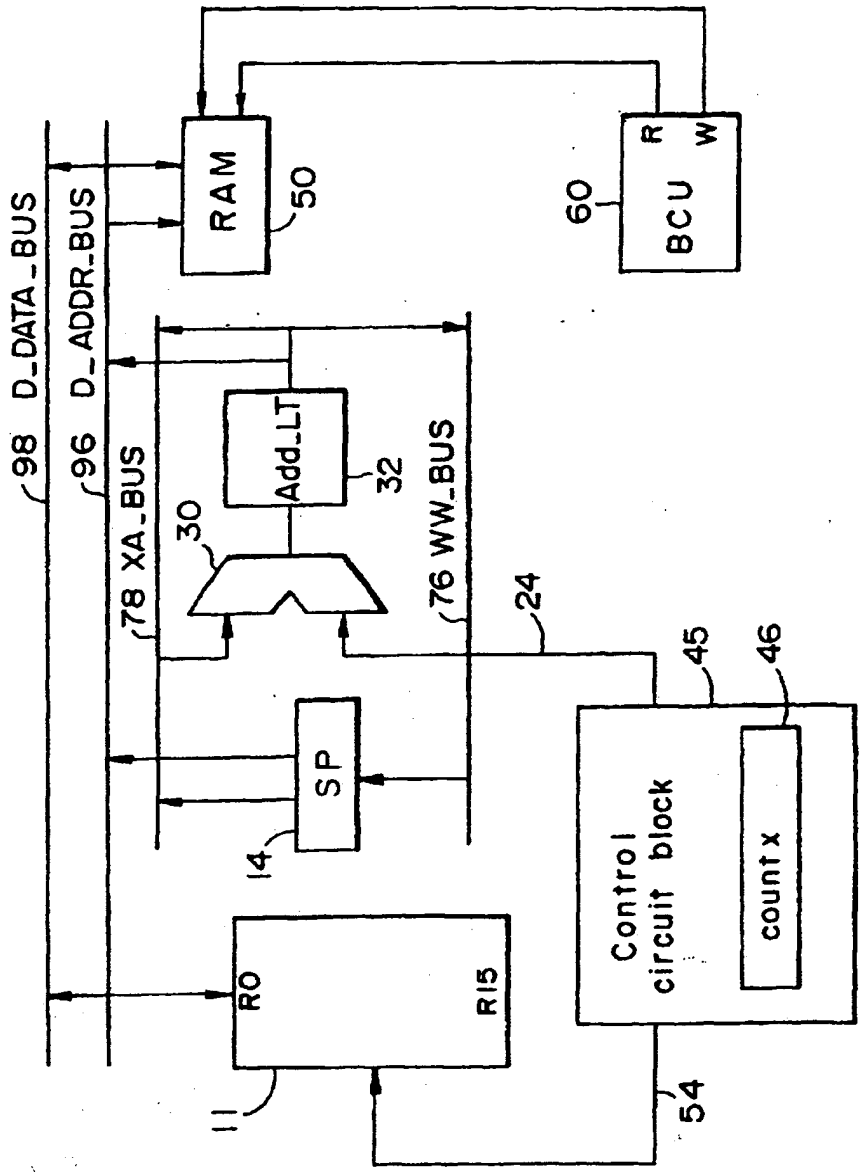

98 D_DATA_BUS
96 D_ADDR_BUS
78 XA_BUS
76 WW_BUS
RAM
50
60
BCU
R
W
Add_LT
32
30
24
45
46
SP
14
Control circuit block
count x
R0
R15
11
54

FIG. 21

Flowchart of pushn execution

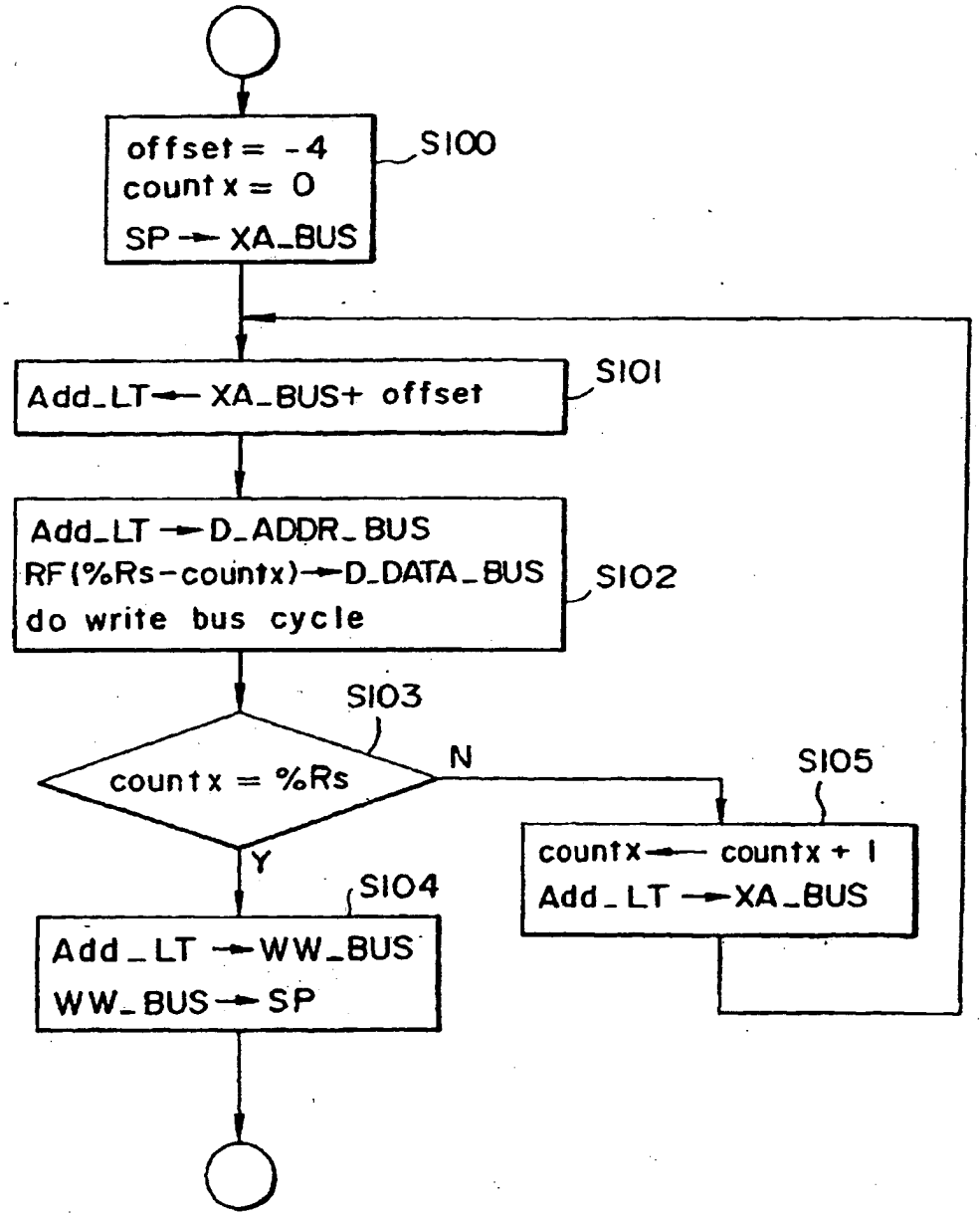


FIG.22

Flowchart of pop execution

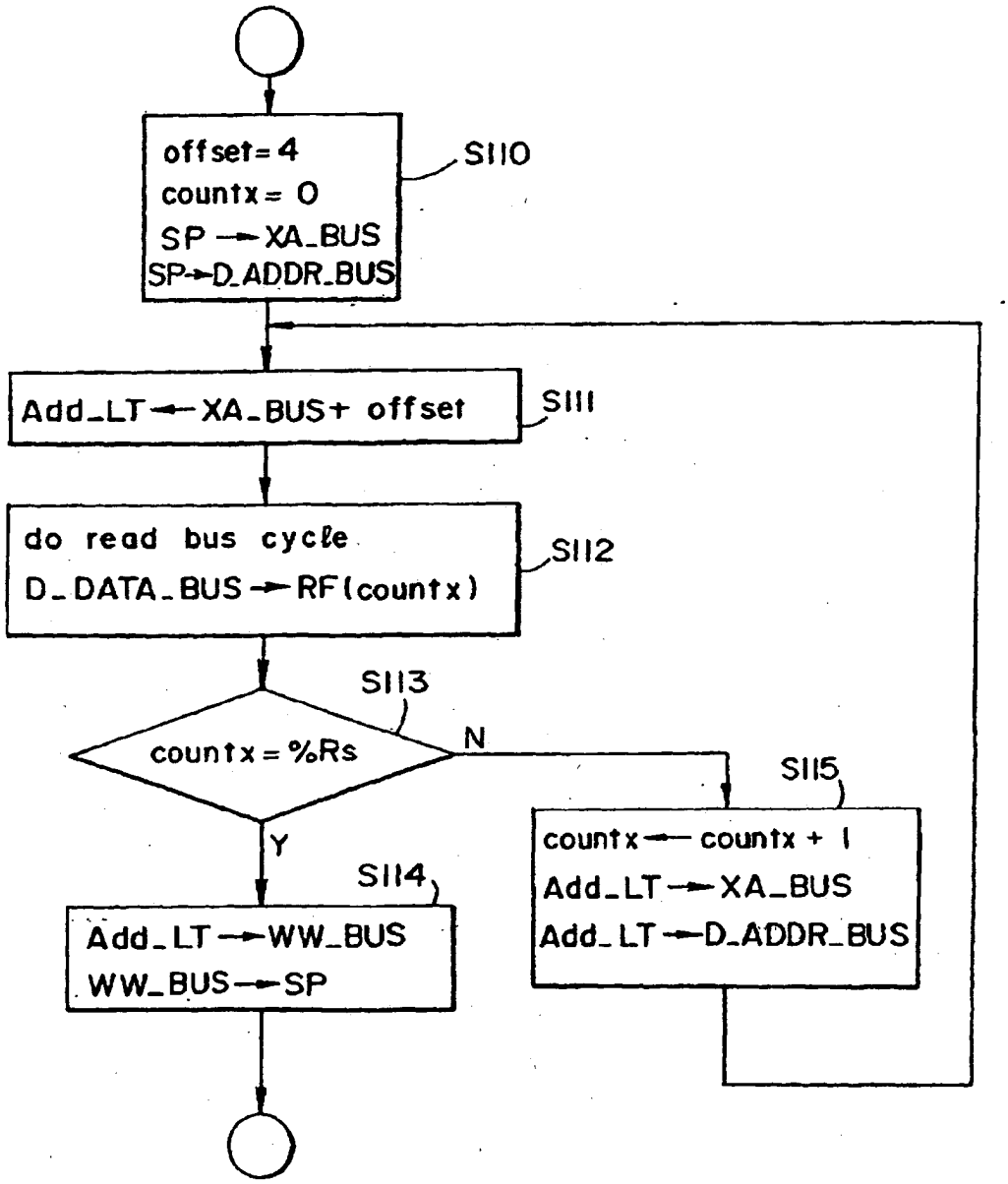
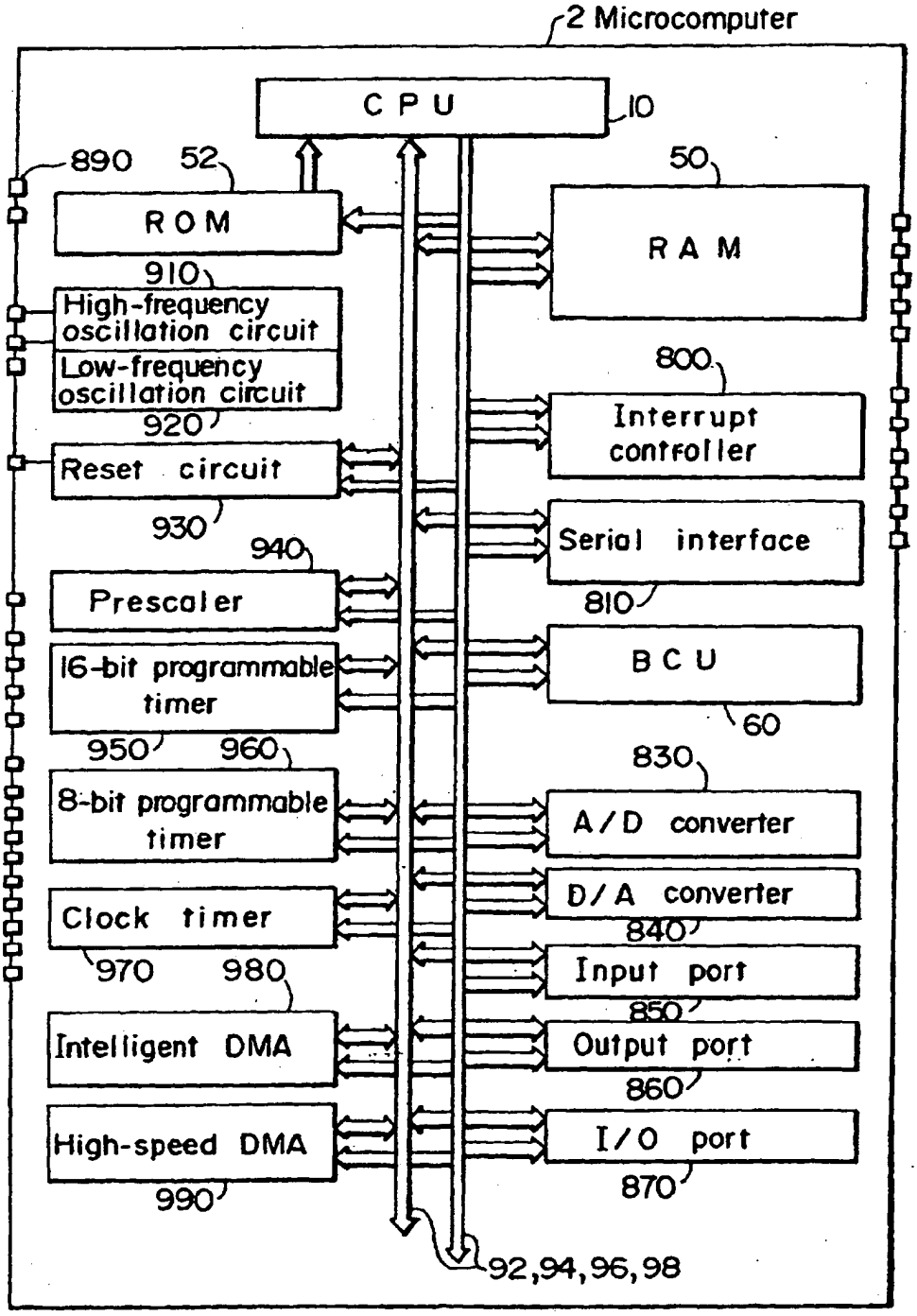


FIG. 23


2 Microcomputer
CPU
10
890
52
50
ROM
RAM
910
High-frequency oscillation circuit
Low-frequency oscillation circuit
920
800
Interrupt controller
Reset circuit
930
940
Serial interface
810
Prescaler
16-bit programmable timer
BCU
60
950
960
830
8-bit programmable timer
A/D converter
D/A converter
840
Clock timer
970
980
Input port
850
Intelligent DMA
Output port
860
High-speed DMA
I/O port
990
870
92,94,96,98